INPRESSCO
International Press Corporation

International Journal of Current Engineering and Technology
E-ISSN 2277 – 4106, P-ISSN 2347 - 5161
©2014 INPRESSCO®, All Rights Reserved
Available at http://inpressco.com/category/ijcet

Research Article

A Study of N-Tunneling Field Effect Transistor (NTFET) through Silvaco TCAD Simulator to Overcome the Technology Limitation of Conventional MOSFET

Praveen Kumar Singh[Ȧ*], Anil Kumar[Ȧ], A.K.Jaiswal[Ȧ], Rajeev Paulus[Ȧ] and Mayur Kumar[Ȧ]

[Ȧ]ECE, SHIATS (Deemed-to-be-university), U.P., India

Accepted 02 June 2014, Available online 20 June 2014, **Vol.4, No.3 (June 2014)**

Abstract

In this paper, it is designed and analyzed the n type tunneling Field Effect Transistor (TFET) to obtain sub-threshold swing parameter (SS) below 60 mV/dec, it is better than the limit of conventional MOSFET. SILVACO TCAD is used for rigorous study of p-i-n structure based on Silicon. It is minimised the short channel effect of SiO_2 material. It is obtained that TFET has good ability to produce high drive current at very low supply voltage (0.1V) with very low leakage current negligible.

Keywords: *TFET, band-to-band tunneling, short channel effect, sub-threshold swing.*

1. Introduction

A Tunneling Field Effect Transistor (TFET) has capability to replace a MOSFET showing better properties over conventional MOSFET. In conventional MOSFET limitation of sub-threshold swing (SS) is limited to 60 mV/dec, while for TFET is below 60 mv/dec at room temperature. On the other hand, the TFET technology has drawback of smaller on current (I_{ON}) as compared to the MOSFET at the same channel length (L_{CH}). It has been proven that the SS parameter of the TFET depends on the gate voltage (V_{GS}), while in case of the MOSFET, it is not function of gate voltage and the physical reason is the large tunneling barrier. TFET operated in the tunneling dominant region where band-to-band tunneling is responsible for drain current. The tunneling mechanism occurs in drift dominant region in case of larger channel resistance (R_{CH}), in turn the drain current produces due to drift mechanism. The tunneling especially band-to-band tunneling (BTBT) for the p-i-n structures have been studied. Compared to the n-i-n MOSFET geometry, the p-i-n tunnel FETs (TFETs) can produce a sharper sub-threshold slope below the MOSFET limit of 60mV/decade at room temperature. This can demonstrate the lower off-current (I_{OFF}) and results lower leakage power (L_{eakage}). The on-current associated with TFET is limitation due to the tunneling barrier, which limits the p-i-n based TFET performance. As compared to n-i-n structure based MOSFETs, p-i-n structure based TFETs have performance advantages in logic circuits. It is free from short channel effects as the channel current is controlled by the tunneling mechanism, while in conventional MOSFET technology suffers from the high short channel effect at lower dimensions.

*Corresponding author: **Praveen Kumar Singh** is a PG student

2. Device Structure and Material Parameters

The structure under consideration is shown in Fig. 1. The device consists SOI type wafer, in which intrinsic type Silicon layer has been deposited. It is supposed that during process of creation of TFET structure, the Silicon layer has been doped p^+-type in less than half and some portion has been protected by mask to create underneath region intrinsic. The remaining silicon region has been doped n^+-type to create p-i-n structure laterally. After doping we have deposit Silicon Oxide material (SiO_2) to minimise the short channel effect. Over oxide material we have deposited poly-silicon for creation of Gate. It is deposited Aluminium over the P^+- silicon, N^+-silicon and over gate for taking the contacts for the biasing purposes named as drain, source and gate contacts.

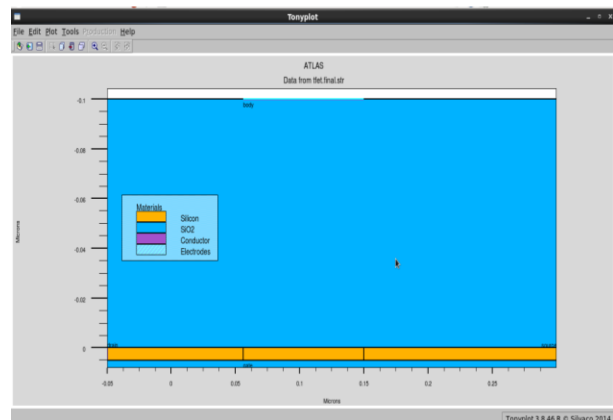

Fig.1: NTFET structure

The Sio_2 region thickness has been taken 300nm while the laterally deposited silicon thickness has been taken 500nm. The doping of n-type silicon has been done by the

generic donors with dose 10^{18} /cm^3, while the middle region has been doped n-type with generic donors with dose 10^{17} /cm^3 and the p^+ silicon region has been doped with acceptor dose 10^{20} /cm^3 as shown in Fig. 2.The standard material parameters have been taken from the SILVACO material database for silicon and oxide materials.

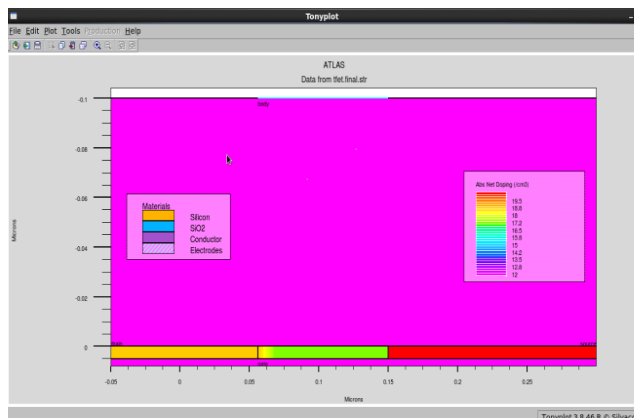

Fig.2: NTFET doping profile

A. Numerical Model

A two-dimensional numerical simulation of a homojunction p-i-n structure based field effect transistor has been done for node generate semiconductor and parabolic shape of conduction band for accurate approximation, which is in good agreement with the numerical solution in the reduced Fermi level range. It has been proved that the omission of carrier degeneracy and conduction band parabolicity will lead to enormous error in the calculation of the drain current NTFET device based on silicon material. The results presented in this work are obtained with ATLAS simulator. The Newton iteration method has been used to solve five nonlinear decoupled equations. The Newton based method improves the efficiency of the iteration.

A program has been developed for simulation of two-dimensional p-i-n FET device based on silicon. The standard formulae used in calculations of band gap energy, effective mass, mobility of charge carriers, electron affinity, SRH, Band to Band tunneling model.

The doping of the regions has been taken analytically uniform for all three regions in the above simulation. Band-to-band standard nonlocal tunneling model has been considered for tunneling mechanism. The surface recombination process at the contacts has been given due to consideration in our simulation of homostructure. The quality of the interface has been characterized in terms of surface recombination velocity.

It has been taken into account the Fermi–Dirac statistics for parabolic shape of conduction band in all the calculations of carrier and doping densities. The standard bandgap narrowing effect has been considered in the analysis.

3. Results & discussions

The schematic energy band diagram of the proposed p-i-n structure based on silicon is shown in Fig. 3. The energy band diagram of heterojunction has been obtained by applying the classical theory of Anderson. From the schematic energy band diagram, it is clear electrons can tunnel from p^+ region to n^+ region as the valance band carriers of p^+ region have high energy as compared to conduction band of n^+ region. The narrow intrinsic region has been chosen to perform tunneling mechanism. The tunneling rate of carriers have been depicted in the Fig. 4a showing the tunneling mechanism is dominant from p^+ region to intrinsic n-type region and Fig.4b, the graphical tunneling rate has been shown that tunneling is dictated under p^+- to n- region.

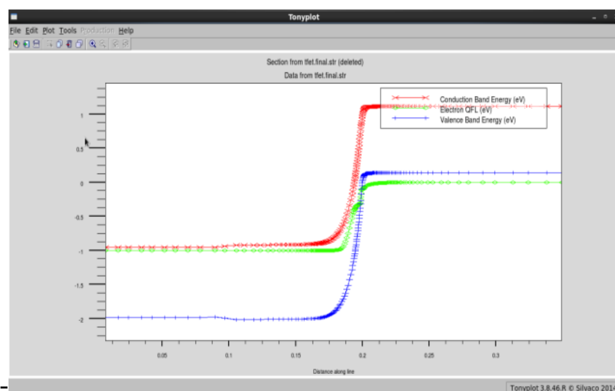

Fig.3: Schematic Band diagram with Fermi level

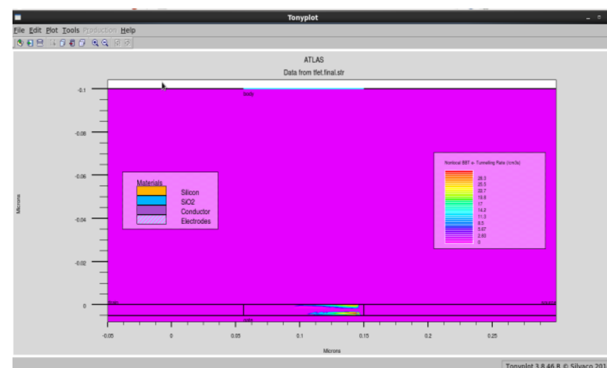

Fig. 4a: Contour of tunneling under the structure

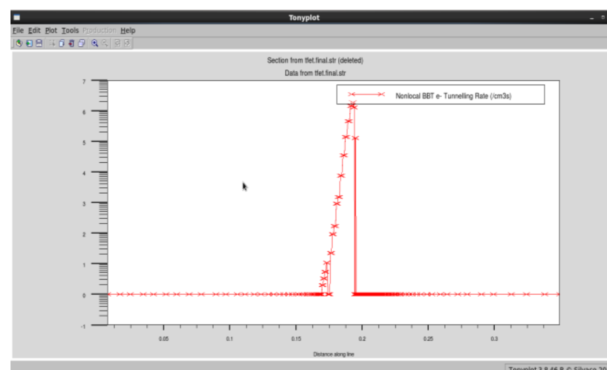

Fig. 4b: Tunneling Rate

The electrical potential in the device structure has been depicted in the Fig. 5 under biasing condition. The

maximum variation in the potential under biasing of drain and gate can be seen at p^+-n interface, where tunnelling mechanism is dominant. The potential variation is responsible for high tunneling of carriers from p^+ region to n^+ region through intrinsic n-type region.

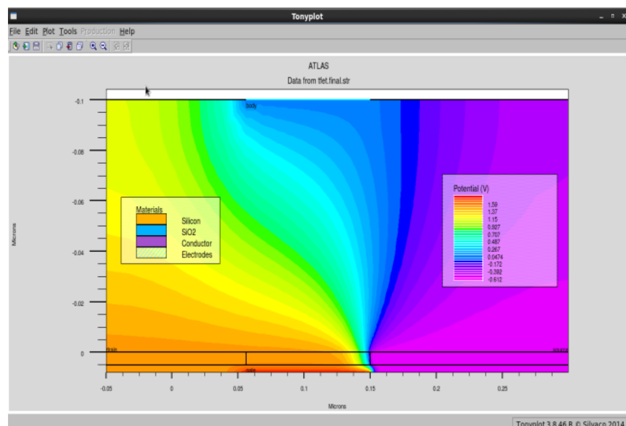

Fig. 5: Contour of Electrical Potential under the structure

Fig. 6 shows the variation in temperature with respect to carrier's product (n*p). Due to tunneling mechanism it is clear from the graph that temperature variation is maximum in the intrinsic n-type region as the carrier tunneling through this region and hence increasing the temperature of the region.

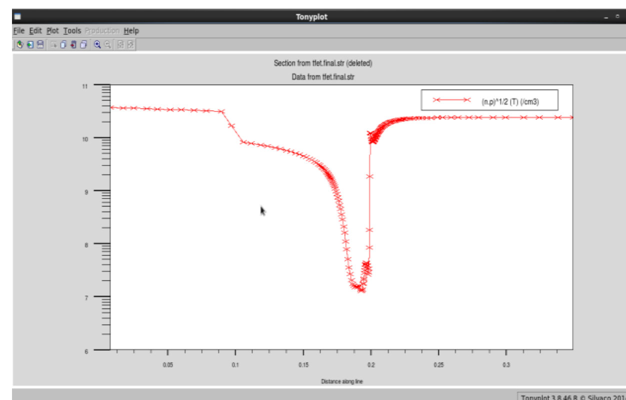

Fig. 6: Effect of tunneling in terms of carriers product and temperature variation due to tunneling mechanism

Fig.7 is shown here as the variation of drain current with respect to gate voltage. The tunneling mechanism has been defined in the region assuming a square slab of dimension 0.1 micron to 0.17 micron in x-axis and 0 to .0049 micron in the y-axis shown above in Fig.1. The simulation used a dynamic nonlocal BTBT model as well as a recombination –generation is also considered for drain current calculation. The tunneling mechanism has been controlled through the application of -0.35V to 1.15 V. However drain voltage has been fixed at 1V. The drain current shown below in fig. 7 that the NTFET reaches in on state at almost near 0.1 V of gate current. As we increase the gate voltage beyond the 0.1 V, drain current increase in almost linear fashion. The I_d-V_G curve shows that the NTFET, which is dictated by tunneling mechanism can be switch into ON state at very low voltage compared to conventional MOSFET which has limitations. Also, as the drain current is produce due to tunneling mechanism, the short channel effect is negligible.

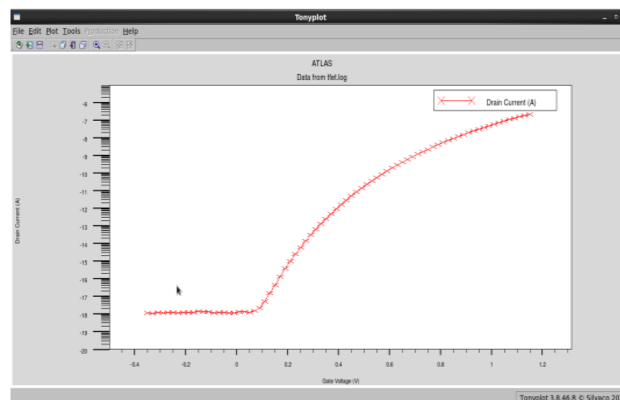

Fig. 7: Variation of drain current with respect to gate voltage

Conclusion

The present study of NTFET shows that at lower voltage we get the lower sub-threshold swing and thereby lower supply voltage needed, in turn reduce the power dissipation. This analysis requires experimental verification to understand the simulated I_d-V_G behaviour and evaluation of the potential of TFET device to replace the existing conventional MOSFET with cost effectiveness.

References

Silvaco Int., Santa Clara, CA, 2010 ATLAS User's Manual A 2-D Numerical Device Simulator.

K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, I-MOS: A novel semiconductor device with a sub-threshold slope lower than kT/q, in *IEDM Tech. Dig.*, 2002, pp. 289–292.

K. E. Moselund, H. Ghoneim, M. T. Bjork, H. Schmid, S. Karg, E. Lortscher, W. Riess, and H. Riel, Comparison of VLS grown Si NW tunnel FETs with different gate stacks, in *Proc. Eur. Solid State DeviceRes. Conf.*, Sep. 2009, pp. 448–451.

R. K. Pandey, K. V. R. M. Murali, S. S. Furkay, P. J. Oldiges, and E. J. Nowak, Crystallographic-orientation-dependent gate-induced drain leakage in nanoscale MOSFETs, *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2098–2105, Sep. 2010.

A. Appaswamy, M. Bajaj, R. Pandey, S. Furkay, and K. Murali, A modified local density approximation based channel quantization model for nanoscale MOSFETs, in *Proc. 15th Int. Workshop Phys. Semicond.Devices*, 2009, pp. 759–762.

K. Boucart and A. M. Ionescu, Double-gate tunnel FET with high-κ gate dielectric, *IEEE Trans. Electron Devices*, vol. 54, no. 7, pp. 1725–1733, Jul. 2007.

K. Bhuwalka, J. Schulze, and I. Eisele, Scaling the vertical tunnel FET with tunnel bandgap modulation and gate work function engineering, *IEEE Trans. Electron Devices*, vol. 52, no. 5, pp. 909–917, May 2005.

N. Patel, A. Ramesha, and S. Mahapatra, Drive current boosting of n-type tunnel FET with strained SiGe layer at source, *Microelectron. J.*, vol. 39, no. 12, pp. 1671–1677, Dec. 2008.

A.C Seabaugh, Qin Zhang, Proceedings of the IEEE, Vol. 98(12), 2010.

Authors

Praveen Kumar Singh is student of M.Tech. ECE (MCE) in the Department of Electronics & Communication Engineering in SHIATS-DU, Allahabad.He received his B.Tech degree from College of Engineering and Rural Technology Meerut, (U.P.) Affiliated to Uttar Pradesh Technical University, Lucknow (U.P.).He is Graduate Student Member of IEEE Member No. 92934616 in Uttar Pradesh section.

Dr. Anil Kumar is Assistant Professor in ECE Department at SHIATS-DU Allahabad. He obtained B.E from MMMEC Gorakhpur in ECE, M.Tech. from IIT BHU Formerly IT B.H.U. Varanasi in Microelectronics Engg. And he has done Ph.D. from SHIATS-DU Allahabad. He guided various projects & research at undergraduate & postgraduate level. He published many research papers in different journals. He has more than 10 years teaching experience and actively involved in research and publications. His area of interest includes Antenna, microwave, artificial neural network and VLSI.

A.K. Jaiswal is Prof. and Head of ECE-Department at SHIATS-Allahabad. He obtained M.Sc. in Tech. Electronics & Radio Engg. from Allahabad University in 1967. He guided various projects & research at undergraduate & postgraduate level. He has more than 40 years Industrial, research and Teaching experience and actively involved in research and publications. His area of interest includes Optical Networks and satellite communication.

Dr. Rajeev Paulus Working as an Assistant Professor in the Department of Electronics and Communication Engineering in SHIATS, Allahabad. He received the degree of M.Tech from MNNIT, Allahabad. He received the degree of Ph.D. from SHIATS, ALLAHABAD. He has presented and published various research papers in national and international Journals and conferences. He is currently focusing on the area of wireless sensor and adhoc network, high speed data network.

Mayur Kumar is Asst. Prof. at SHIATS-DU Allahabad. He obtained B.E from North Maharastra University in Electronics Engineering, M.Tech. from SHIATS-DU Allahabad in communication System Engineering. He has more than 10 years teaching. Experience and actively involved in research and publications.