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Research Article

Design of Flip-Flops for High Performance VLSI Applications using Deep Submicron CMOS Technology

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Abstract

This paper enumerates low power, high speed design of SET, DET, TSPC and C2CMOS Flip-Flop. As these flip flop topologies have small area and low power consumption, they can be used in various applications like digital VLSI clocking system, buffers, registers, microprocessors etc. The Flip-Flops are analyzed at 90nm technologies. The above designed Flip-Flops and Latches are compared in terms of its area, transistor count, power dissipation and propagation delay using DSCH and Microwind tools. As chip manufacturing technology is suddenly on the threshold of major evaluation, which shrinks chip in size and performance is implemented in layout level which develops the low power consumption chip using recent CMOS micron layout tools. This project proposes low power high speed design of flip flops in which True Single Phase Clocking (TSPC) and C2CMOS flip flop compared with existing flip flop topologies in term of its area, transistor count, power dissipation, propagation delay, parasitic values with the simulation results in microwind.

Keywords: *CMOS, flip-flop topologies, power dissipation, propagation delay and transistor count.*

1. Introduction

For high performance VLSI chip-design, the choice of the back-end methodology has a significant impact on the design time and the design cost. Latches and flip-flops have a direct impact on power consumption and speed of VLSI systems. Therefore various following flip flop topologies were designed for some dedicated applications.

Flip-Flop is an electronic circuit that stores a logical state of one or more data input signals in response to a clock pulse. For submicron CMOS technology area, topology selection, power dissipation and speed are very important aspect especially for designing Clocked Storage Element (CSE) for high-speed and low-energy design like portable batteries and microprocessors. Various classes of flip-flops have been projected to achieve high-speed and low-energy operation. A flip-flop is a bistable circuit which stores a logic state of 0 or 1 in response to a clock pulse with one or more data inputs. In digital circuit design, large proportion contributes to synchronous design and they are operated based on the clock signal to reduce the complexity of the circuit design. Design of some flip flop architectures and analyse it in term of power consumptions, area and propagation delay.

Flip-flops are often used in computational circuits to operate in selected sequences during recurring clock intervals to receive and maintain data for a limited time period sufficient for other circuits within a system to further process data. Following are most high performance flip flops.

[1] Single Edge-Triggered Flip-Flop (SET)
[2] Double Edge-Triggered Flip-Flop (DET)
[3] True Single-Phase-Clock Flip-Flop (TSPC)
[4] Clocked CMOS Flip-Flop (C2CMOS)

At each rising or falling edge of a clock signal, the data stored in a set of Flip-Flops is readily available so that it can be applied as inputs to other combinational or sequential circuitry. Such flip-flops that store data on both the leading edge and the trailing edge of a clock pulse are referred to as double-edge triggered Flip-Flops otherwise it is called as single edge triggered Flip-Flops.

In digital CMOS circuits there are three sources of power dissipation, the first is due to signal transition, the second comes from short circuit current which flows directly from supply to ground terminal and the last is due to leakage currents. As technology scales down the short circuit power becomes comparable to dynamic power dissipation. Furthermore, the leakage power also becomes highly significant. High leakage current is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length and gate oxide thickness are reduced. When technology scales down, total power dissipation will decrease and at the same time delay varies depends upon supply voltage, threshold voltage, aspect ratio, oxide thickness, load capacitance.

In this paper, the listed architecture of D Flip-Flop is designed and verified using Microwind simulation tools.

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The paper is organized as the discussion on previously designed architecture and compares all the flip flop circuit in terms area, power dissipation, transistor count and propagation delay. Elucidation of flip flop topologies in section-I discussed the architecture and detail operation of it. Section-III gives details about the simulation results and comparison. Section-IV concludes the paper.

2. Elucidation of Flip-Flop Topology

2.1 Efficient architecture of SET D flip flop

The efficient architecture of Single Edge Trigger flip flop which is based on negative edge trigger given in following figure1. In that when *clock* is high; the master latch is updated to a new value of the input *D*. The slave latch produces the previous value of *D* on the output *Q*. When *clock* goes down, the master latch turns to memory state. The slave circuit is updated. The change of the clock from 1 to 0 is the active edge of the clock. This type of latch is a negative edge flip flop.

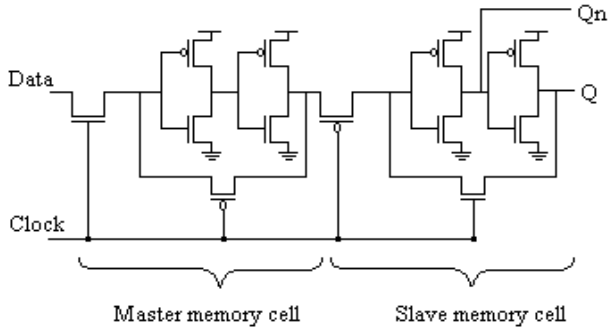

Figure 1: Efficient architecture of SET D flip flop

The reset function is added by a direct grounding the input signal present at feedback path of the master and slave memories, using nMOS devices. This added circuit is equivalent to an asynchronous Reset, which means that *Q* will be reset to 0 when *Reset* is set to 1, without waiting for an active edge of the clock. The above structure is drawn with the help of DSCH tool represented into cmos and passes transistor logic shown in figure 4.

2.2 Double Edge-Triggered Flip-Flop (DET)

Double edge- triggered (DET) flip-flop which samples the input data by both the clock's rising edge and falling edge. Figure 2 specifies the principles of DET flip-flop design and presents a logic structure based on multiplexors (MUX), which is used to realize this type of flip-flop. This flip-flop is basically a Master Slave flip-flop structure which has two data paths. The upper data path consists of a Single Edge Triggered flip-flop implemented using PMOS pass transistor, this works on negative edge. The lower data path consists of a positive edge triggered flip-flop implemented using NMOS pass transistor. Both the data paths have feedback loops connected such that, in the feedback loop two inverters are connected back to back and in that feedback path one transistor is connected which acts like as a switch whenever the clock is inverted, such that the respective pass transistor of that path is in 'OFF' (open) state then logic level at feedback is retained due to closing of that switch and the retained value is pass to the output through output pass transistors. At output node the inverter is connected to get the output 'Q'. Figure 2 is the schematic is of Double Edge trigger flip flop drawn with the help of Dsch tool.

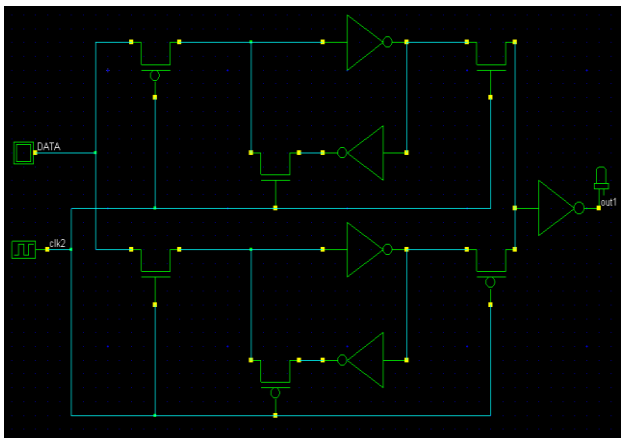

Figure 2: Schematic of DET D flip flop in Dsch.

A given schematic of Double edge trigger flip flop is drawn in layout structure with the help of Microwind simulation tool. In these dual edge trigger flip flop circuit we use only three metal layers for designing these circuit in layout structure. We had mentioned three label for given layout which is data signal as input to the circuit while enabling the input, clock signal is applied to gate terminal of respective pass transistor and for viewing output we have to connect view nodes Q (output) as shown in the following figure 8. The layout is designed at 90nm foundry level 6 metal copper- strained SiGe Lowk (1.2V-2.5V).

2.3 True Single-Phase-Clock Flip-Flop (TSPC)

A common dynamic flip-flop variety is the true single-phase clock (TSPC) type which performs the flip-flop operation with little power and at high speeds. However, dynamic flip-flops will typically not work at static or low clock speeds: given enough time, leakage paths may discharge the parasitic capacitance enough to cause the flip-flop to enter invalid states. The architectures of True single phase clock flip flop based on edge triggering i.e. positive, negative and positive edge triggered using split output latches. From the three architectures we consider negative edge trigger for dynamic latches are currently the principle design style for high speed digital circuits. In CMOS, with edge-triggered storage elements, would we want negative edge-triggered or positive edge-triggered? Typically, want the clock edges as sharp as possible. Because *n*MOS devices provide stronger pulldown, usually use negative edge-triggered devices in CMOS.

As Negative Edge trigger architecture is selected for our TSPC flip flop in that CMOS based circuit the first stage is Non precharged N then output of that is applied as input to the Precharged P stage and at last the outp$\overline{Q}$ of these is given to Non precharged P stage output of

these stage is then complement it by simply connected invert at the output side which shown in following figure 3: now for resetting the

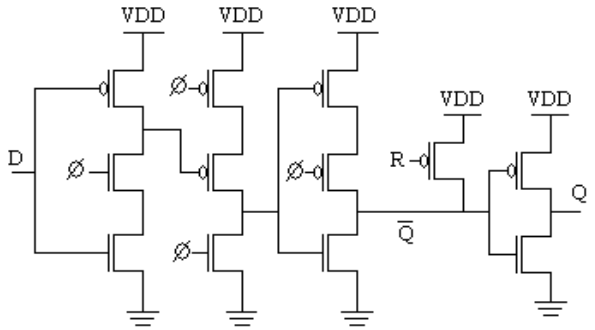

Figure 3: Negative Edge Trigger TSPC flip flop

Negative edge TSPC circuit we connect one PMOS transistor at the output stage of non precharged P stage it connected between VDD and the output path of flip flop. The single phase of clock is applied to the all the stages of below TSPC flip flop so that it is known as True Single Phase Clock Flip flop. Total 12 transistors are required for following circuit including resetting logic.

2.4 Clock 2 CMOS Flip flop architecture (C2CMOS):-

An ingenious negative edge-triggered register that is based on a master-slave concept insensitive to clock overlap is shown in figure 4. This circuit is called the C2CMOS (Clocked CMOS) flip-flop which operates in two phases: when clk=1, the first driver is turned on, and the master stage acts as an inverter sampling the inverted version of D. The master stage is in the evaluation mode. When clk=0, the master stage section is in hold mode, while the second section evaluates. The previous value stored is propagated to the output node through the slave stage, which acts as an inverter.

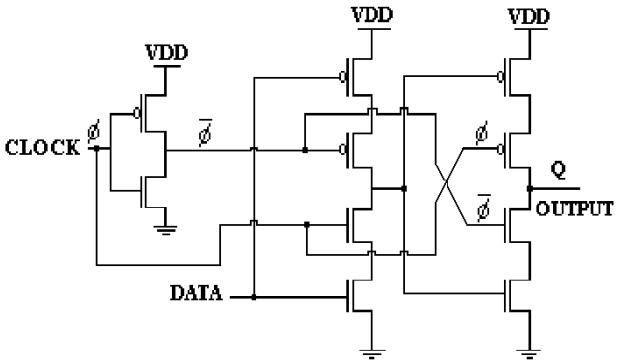

Figure 4: C2CMOS Flip flop architecture.

The above circuit diagram is of clock 2 CMOS flip flop topologies in that the data signal is applied to upper PMOS transistors lower NMOS transistor of the first stage of flip flop, clock signal Ø is applied to NMOS of first stage & PMOS transistor of second stage of circuit and its inverted clock signal is applied to PMOS transistor of first stage & NMOS transistor of second stage. The output of the first stage is applied as input to the second stage of architecture the Output of C2CMOS flip flop is getting at the node 'Q'.

3. Results And Discussions

The structure is negative edge trigger flip flop drawn with the help of DSCH tool represented into cmos and passes transistor logic shown in figure 5.

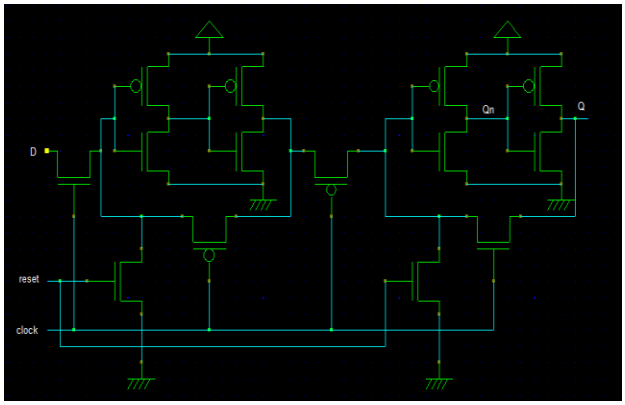

Figure 5: Schematic of SET D flip flop in Dsch.

Above schematic of negative edge trigger flip flop is drawn in layout structure with the help of Microwind simulation tool. In these single edge trigger layout designed circuit we use only three metal layers for designing these circuit in layout structure. When we want to reset the flip flop we applied clock signal high as source to that node, as shown in the following figure 6.

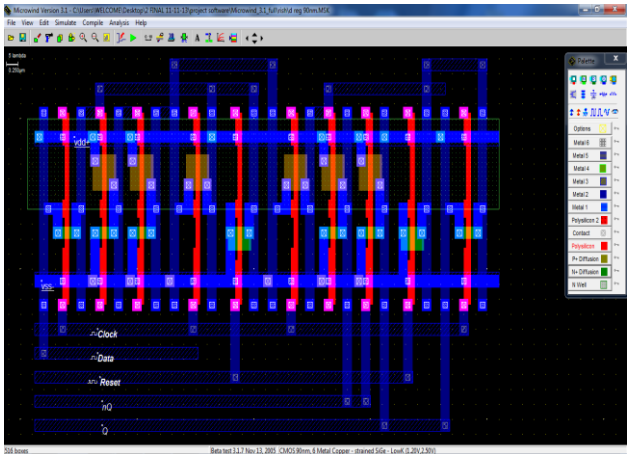

Figure 6: Single Edge Trigger Flip-flop Layout Design

After complete design, the layout is check with DRC whether there is any violation in designed layout, if the layout is ok then we simulate the layout structure after simulation we get output as shown in following figure 7.

Simulation output of the single edge trigger flip flop as shown in above figure. In these simulation when reset signal is high the output goes 'low' which implies that whatever the input is present directly grounded through NMOS transistor in master and slave cell. From the simulation it clear that the output 'Q' follows the input 'D' at negative (falling) edge and 'nQ' is complement of 'Q'.

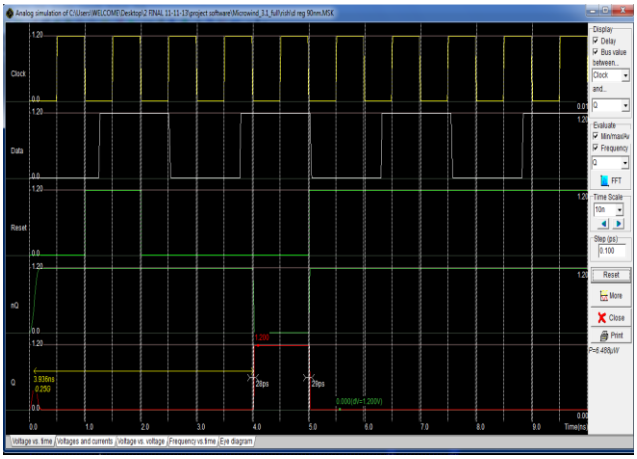

Figure 7: Single Edge Trigger Flip-flop simulation output

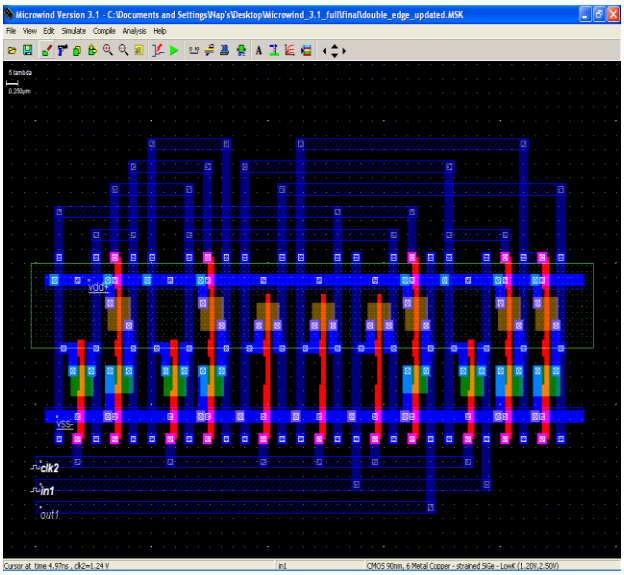

Figure 8: Double Edge Trigger Flip-flop Layout Design

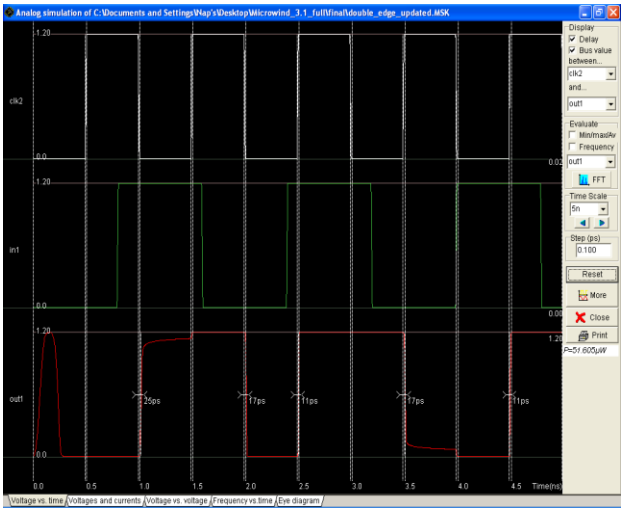

Figure 9: Double Edge Trigger Flip-flop simulation output

Simulation output of the double edge trigger flip flop as shown in above figure 9. From the simulation graph we can say that both the edges of the clock are well utilized by the designed layout. The total power required by the DET flip flop is 51.60µw, operates on 1.2V and the propagation delay is of 11ps. Though DET flip flop required more power but switching is fast as compare with SET.

The Schematic of TSPC circuit is drawn with the help of Dsch simulation tools, schematic of negative edge trigger TSPC flip flop is as given in following figure 10.

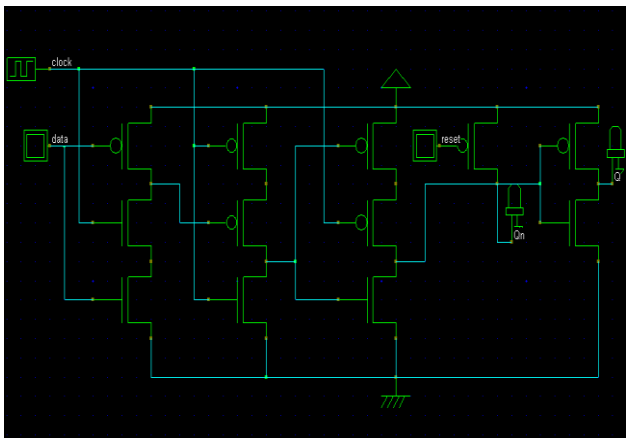

Figure 10: Schematic of TSPC D flip flop in Dsch.

Above schematic of negative edge trigger TSPC flip flop is drawn in layout structure with the help of Microwind simulation tool. In TSPC flip flop circuit we use only three metal layers for designing these circuit in layout format. We had mentioned five label for given layout which is data signal as input to the circuit while enabling the input, clock signal is applied to gate terminal of respective clock transistor of precharged or non precharged stage and for viewing output we connect two view nodes Q (output) and Qn, for resetting the flip flop we connect one PMOS transistors which is in between VDD and output path before inverter. When we want to reset the flip flop we applied clock signal low as source to that R node, as shown in the following figure 11. The layout is designed at 90nm foundry level 6 metal copper- strained SiGe Lowk (1.2V-2.5V).

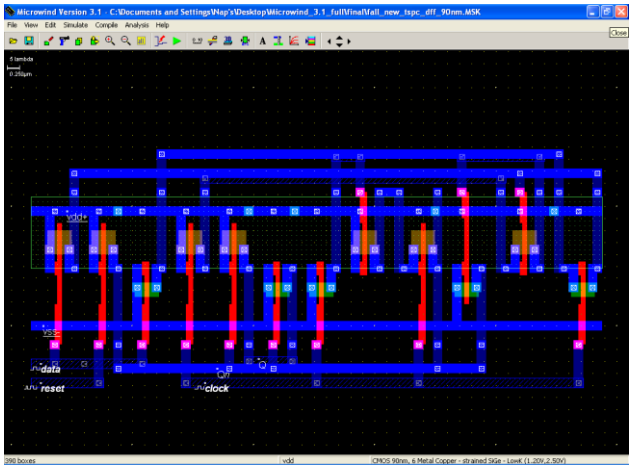

Figure 11: TSPC D Flip-flop Layout Design.

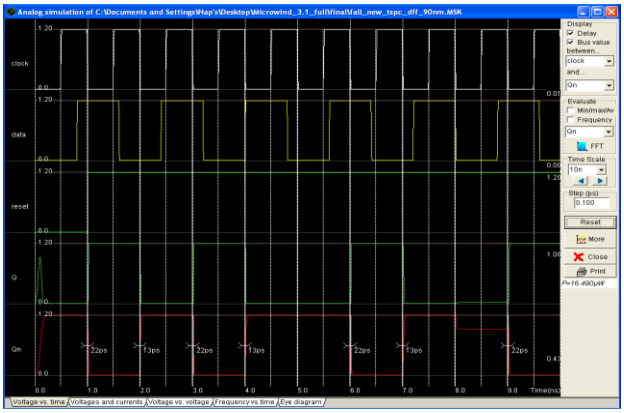

Figure 12: TSPC D Flip-flop simulation output.

From the simulation it clear that the output 'Q' follows the input 'D' at negative (falling) edge and 'nQ' is complement of 'Q'. The total power required by the TSPC flip flop is 16.49µw is very low as compared with other architectures, it operates on 1.2V and the propagation delay is of 13ps.

The Schematic of above CMOS circuit figure 4 is drawn with the help of Dsch simulation tools, schematic of C2CMOS flip flop is as given in following figure 13.

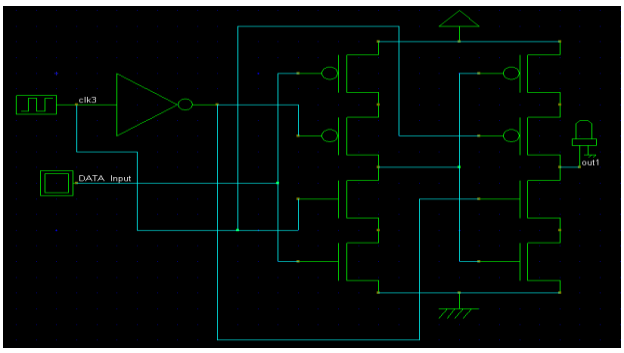

Figure 13: Schematic of C2CMOS D flip flop in Dsch.

Above schematic of C2CMOS flip flop is drawn in layout structure with the help of Microwind simulation tool. When the input D is '1' and clock is '1' then master stage is ON & slave is OFF, when input D is '0' and clock is '0' then master stage is OFF & slave is ON

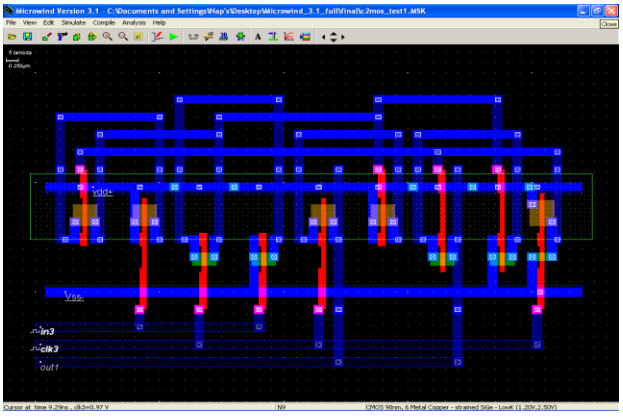

Figure 14: C2CMOS Flip-flop Layout Design.

In above C2MOS layout design we used only three metal layers and the complete design required only 10 transistors which is less as compares with other.

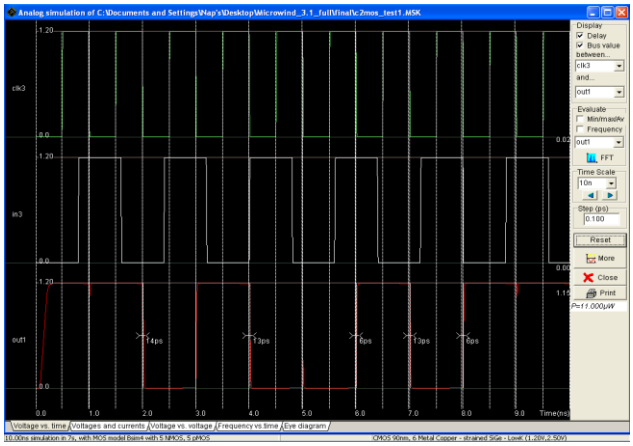

Figure 15: C2CMOS Flip-flop simulation output.

Simulation output of the C2CMOS flip flop as shown in above figure 15. From the simulation it clear that the output 'Q' follows the input 'D' at negative (falling) edge of the clock. The total power required by the C2CMOS flip flop is 11µw is very low as compared with other architectures, it operates on 1.2V and the propagation delay is of 6ps.

Table 1 Performance Comparison of Flip-Flop topologies

Architecture	**SET**	**DET**	**C2CMOS**	**TSPC**
Technology	CMOS 90nm, 6 Metal Copper- strained SiGe Lowk (1.2V-2.5V).			
Voltage Rating	1.20 V			
Power Dissipation (µW)	6.48	51.60	11	16.49
Propagation Delay (ps)	28	11	6	13
Area (µm^2)	57.77	75.62	49.92	55.22
Transistors	14	16	10	12

From above comparisons the analysis shows that total power required by the SET flip flop is 6.48µw is very low as compared with other architectures, it operates on 1.2V and the propagation delay is of 28ps. The Double Edge Trigger flip flop architecture utilizes both edges of the clock as compared with SET, C2CMOS and TSPC. The total power required by the DET flip flop is 51.60µw and the propagation delay of the double edge trigger flip flop is 11ps which minimum as compares with SET and TSPC. Though DET flip flop required more power but switching is fast as compare with SET.

Design of TSPC flip-flop shows better performance in terms of propagation delay, power dissipation and area i.e. only 12 transistor required for given TSPC flip flop which is less as compared with SET and DET, only single edge of clock phase required for all the stages operates at only one edge in present research.

Design of C2CMOS D flip-flop shows better performance in terms of propagation delay, power dissipation and area i.e. only 10 transistor required for given C2CMOS flip flop. C2CMOS and TSPC flip flop architecture shows better result on given key parameters compared with SET and DET.

4. Conclusions

In this paper, an exhaustive analysis and design methodology for commonly used high-speed flip-flops topologies in 90nm CMOS technologies has been carried out. The comparison has been performed with area, delay and power dissipation. The impact of layout parasitic has been included in the transistor-level design phase. The flip-flops chosen for a thorough comparative analysis, whose results are reported in section II and III. According to the presented results, the fastest topology are the C2CMOS and DET since the delay, with respect to area and number of transistor count TSPC and C2CMOS are better while with respect to power dissipation SET shows better result, the best low-power flip-flops are the SET. Moreover, the best topology under clock skew and less propagation delay are DET and C2CMOS.

We conclude that efficient design architecture based on power dissipation, propagation delay and transistor counts for portable applications are TSPC, SET, DET and C2CMOS Flip-flop. Considerate the suitability of flip-flops and selecting the best topology for a given application is an important issue; the low power design SET is suitable for portable applications.

Above performance comparison shows that the C2CMOS and TSPC flip flop architecture shows better result on given key parameters compared with SET and DET. This means that both architectures are suitable in low power, fast switching and minimum area applications.

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