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Research Article

Performance Analysis of Various Switching Scheme in Multilevel Inverters using MATLAB/SIMULINK

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Abstract

In this paper the comparison has been made between the diode clamped multilevel inverter, the flying capacitor multilevel inverter, the cascaded H-bridge multilevel inverter and the two-level inverter. These comparisons are done with respect to losses, cost to benefit ratio, weight and THD. For these comparisons all of the inverters are simulated in MATLAB/SIMULINK. Moreover a goal is to compare three different switching schemes for inverter.

Keywords: *Performance Analysis,MATLAB/SIMULINK, Switching Scheme etc.*

1. Introduction

The power in the battery is in DC mode and the motor that drives the wheels usually uses AC power, therefore there should be a conversion from DC to AC by a power converter. Inverters can do this conversion. The simplest topology that can be used for this conversion is the two-level inverter that consists of four switches. Each switch needs an anti-parallel diode, so there should be also four anti parallel diodes. There are also other topologies for inverters. A multilevel inverter is a power electronic system that synthesizes a sinusoidal voltage output from several DC sources. These DC sources can be fuel cells, solar cells, ultra capacitors, etc (Qamar Alam, 2008). The main idea of multilevel inverters is to have a better sinusoidal voltage and current in the output by using switches in series. Since many switches are put in series the switching angles are important in the multilevel inverters because all of the switches should be switched in such a way that the output voltage and current have low harmonic distortion. Multilevel inverters have three types. Diode clamped multilevel inverters, flying capacitor multilevel inverters and cascaded H-bridge multilevel inverter. The THD will be decreased by increasing the number of levels. It is obvious that an output voltage with low THD is desirable, but increasing the number of levels needs more hardware, also the control will be more complicated. It is a tradeoff between price, weight, complexity and a very good output voltage with lower THD.

Multilevel topologies are able to generate better output quality, while operating at lower switching frequency. This implies lower switching dissipation and higher efficiency. Moreover, this topology utilizes switches with lower breakdown voltage; therefore, it can be used in higher power applications at lower cost. It is worth mentioning that although the number of switches in this approach is higher than other two level topologies, for a sufficient high number of levels, the output filter can be avoided which means less weight, cost and space. On the other hand, even with the same size of filter at the output, the switching frequency can be decreased which means higher efficiency. In general, a greater number of switches in multilevel converters can be justified since the semiconductor cost decreases at a much greater rate than the filter components cost (Fang Z. Peng, 2001; Mohammadreza Derakhshanfar, 2010).

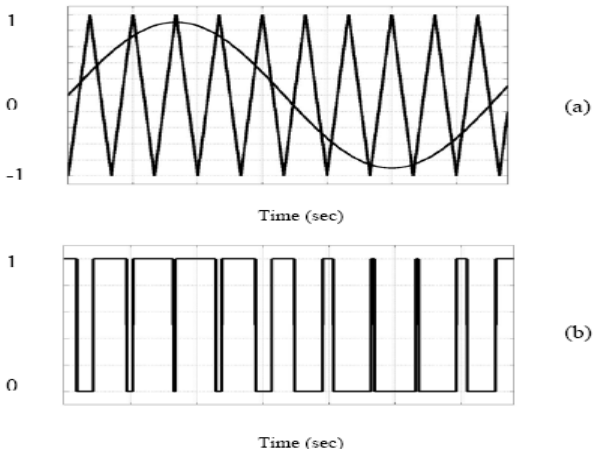

Figure 1: PWM Illustration by the Sine-Triangle Comparison: (a) Sine-Triangle Comparison (b) Switching Pulses

As in the single phase voltage source inverters PWM technique can be used in three-phase inverters, in which three sine waves phase shifted by 120° with the frequency

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of the desired output voltage is compared with a very high frequency carrier triangle, the two signals are mixed in a comparator whose output is high when the sine wave is greater than the triangle and the comparator output is low when the sine wave or typically called the modulation signal is smaller than the triangle. This phenomenon is shown in Figure 1 as is explained the output voltage from the inverter is not smooth but is a discrete waveform and so it is more likely than the output wave consists of harmonics, which are not usually desirable since they deteriorate the performance of the load, to which these voltages are applied (L. M. Tolbert, 1997; K. T. Chau, 2002).

Recent advances in power electronics have made the multilevel concept practical. In fact, the concept is so advantageous that several major drives manufacturers have obtained recent patents on multilevel power converters and associated switching techniques. It is evident that the multilevel concept will be a prominent choice for power electronic systems in future years, especially for medium-voltage operation. Multi-level inverters are the modification of basic bridge inverters. They are normally connected in series to form stacks of level. The number of levels in an inverter bridge defines the number of direct current (DC) voltage steps that are required by the inverter bridge in order to achieve a certain voltage level at its output. Because power semiconductor switches have limited voltage capability, the total DC bus voltage of an inverter bridge is divided into a number of voltage steps, such that each voltage step can be handled by one power switch. For high power applications, voltages and currents must be pushed up. Hence, maximum ratings of power semiconductors become a real handicap. Paralleling devices, subsystems and systems leads to higher current levels. On the other hand, series connections are the solution for dealing with larger voltages. Nevertheless, given a chain of devices connected in series, achieving static and dynamic voltage sharing among switches become a problem. This will also affect the reliability of the system. An advantage of multilevel inverters compared with the classical two- level topology, is that the output voltage spectra are significantly improved due to having a greater availability of voltage levels, Hence, the output voltages can be filtered with smaller reactive components, and additionally, the switching frequencies of the devices can be reduced. These two benefits, together with the ability to deal with higher voltage levels, confer on multilevel inverters a very important role in the field of high power applications. The intriguing feature of the multilevel inverter structures is their ability to scale up the kilovolt-ampere (KVA) rating and also to improve the harmonic performance greatly without having to resort to PWM techniques. The key features of a multilevel structure follow: (Mohammadreza Derakhshanfar, 2010)

- The output voltage and power increase with number of levels. Adding a voltage level involves adding a main switching device to each phase.
- The harmonic content decreases as the number of levels increases and filtering requirements are reduced.
- With additional voltage levels, the voltage waveform has more free-switching angles, which can be reselected for harmonic elimination.
- In the absence of any PWM techniques, the switching losses can be avoided. Increasing output voltage and power does not require an increase in rating of individual device.
- Static and dynamic voltage sharing among the switching devices is built into the structure through either clamping diodes or capacitors.
- The switching devices do not encounter any voltage-sharing problems. For this reason, multilevel inverters can easily be applied for high-power applications such as large motor drives and utility supplies.
- The fundamental output voltage of the inverter is set by the dc bus voltage Vdc, which can be controlled through a variable dc link.

Several combinational designs have also emerged some involving cascading the fundamental topologies. These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels. The most actively developed of multilevel topologies are listed in Figure 2 (Dhana Prasad Duggapu, 2012; M.S Jamil Asghar, 2004; Jose Rodriguez, 2002).

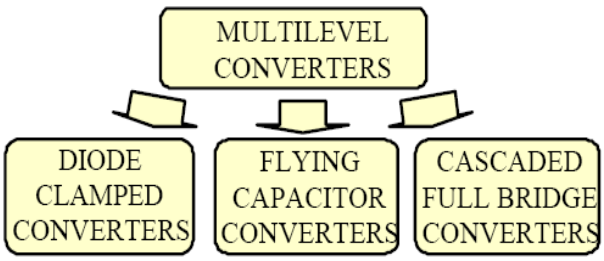


Figure 2: Multilevel Converter Topologies

All three multilevel inverters can be used in reactive power compensation without having the voltage unbalance problem. Table 1 compares the power component requirements per phase leg among the three multilevel voltage source inverter mentioned below. It shows that the number of main switches and main diodes, needed by the inverters to achieve the same number of voltage levels. Clamping diodes were not needed in flying-capacitor and cascaded-inverter configuration, while balancing capacitors were not needed in diode clamp and cascaded-inverter configuration. Implicitly, the multilevel converter using cascaded-inverters requires the least number of components (M.S Jamil Asghar, 2004; Mohammadreza Derakhshanfar, 2010).

2. Modulation Topologies of Multilevel Inverter

The multilevel topology involves several modulation techniques. Each technique involves different modulation methods. The well-known modulation topologies for multi-level inverters as follows: (Jose Rodriguez, 2002)

- Sinusoidal or Sub harmonic Natural Pulse Width Modulation (SPWM).

Table 1: Comparison of Power Component Requirements per Phase Leg among Three Multilevel Inverters.

Inverter Configuration	Diode Clamped	Flying – Capacitors	Cascaded– inverter
Main switching devices	2 (m–1)	2(m–1)	2(m–1)
Main diodes	2 (m–1)	2(m–1)	2(m–1)
Clamping diodes	(m–1)*(m–2)	0	0
DC bus capacitors	(m – 1)	(m – 1)	(m – 1)/2
Balancing Capacitors	0	((m – 1)*(m – 2))/2	0

- Selective Harmonic Eliminated Pulse Width Modulation (SHE PWM) or Programmed-Waveform Pulse
- Width Modulation (PWPWM).
- Optimized Harmonic Stepped-Waveform Technique (OHSW).

The advent of the transformer less multilevel inverter topology has brought forth various pulse width modulation (PWM) schemes as a means to control the switching of the active devices in each of the multiple voltage levels in the inverter. The most efficient method of controlling the output voltage is to incorporate pulse width modulation control (PWM control) within the inverters. In this method, a fixed D.C. input voltage is supplied to the inverter and a controlled A.C. output voltage is obtained by adjusting the on and–off periods of the inverter devices. Voltage-type PWM inverters have been applied widely to such fields as power supplies and motor drivers. This is because: (1) such inverters are well adapted to high-speed self-turn-off switching devices that, as solid-state power converters, are provided with recently developed advanced circuits; and (2) they are operated stably and can be controlled well (M.S Jamil Asghar, 2004; Jose Rodriguez, 2002).

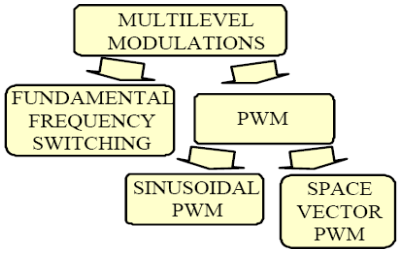


Figure 3: Multilevel Modulation Techniques

From the above all mentioned PWM control methods, the Sinusoidal pulse width modulation (SPWM) is applied in the proposed inverter since it has various advantages over other techniques. Sinusoidal PWM inverters provide an easy way to control amplitude, frequency and harmonics contents of the output voltage. Sinusoidal pulse width modulation (SPWM) is one of the primitive techniques, which are used to suppress harmonics presented in the quasi-square wave. In the modulation techniques, there are two important defined parameters: (Jose Rodriguez, 2002; Mohammadreza Derakhshanfar, 2010).

a. the ratio $P = f_c/f_m$ known as frequency ratio, and
b. the ratio $M_a = A_m/A_c$ known as modulation index,

Where fc is the reference frequency, fm is the carrier frequency, Am is reference signal amplitude and Ac is carrier signal amplitude. For NPC multilevel inverters, most carrier based modulation strategies derive from disposition techniques developed by Carrara et al, where for an M level inverter, M_1 carriers of identical frequency and amplitude are arranged to occupy contiguous bands between $+V_{DC}$ and $-V_{DC}$. These carriers can be arranged in: (M.S Jamil Asghar, 2004)

- Alternative Phase Opposition Disposition (APOD), where each carrier is phase shifted by 1800 from its adjacent carriers.
- Phase Opposition Disposition (POD) where the carriers above the reference zero point is out of phase with those below the zero point by **1800.**
- Phase Disposition (PD) where all carriers are in (Jose Rodriguez, 2002).

3. Multilevel Inverters

This thesis compares three different topologies of inverters (one level inverter, Diode clamped inverter, Flying capacitor clamped inverter and Cascaded H-bridge inverter) Multilevel inverters have three types (Jose Rodriguez, 2002; Mohammadreza Derakhshanfar, 2010).

1. Diode Clamped multilevel inverters
2. Flying Capacitor multilevel inverters
3. Cascaded H-bridge multilevel inverters

4. Basic Principle Of Operation Of Cascaded Multilevel Converters

The Cascaded Multilevel Converters (CMC) is simply a number of conventional two-level bridges, whose AC terminals are simply connected in series to synthesize the output waveforms. Figure 4(a) shows the power circuit for a five-level inverter with two cascaded cells. The CMC needs several independent DC sources which may be obtained from batteries, fuel cells or solar cells (Akihiro Oi, 2005).

Through different combinations of the four switches of each cell, each converter level can generate three different voltage outputs, $+V_{dc}$, 0, $-V_{dc}$. The AC output is the sum of the individual converter outputs. The number of output phase voltage levels is defined by n = 2N+1, where N is the number of DC sources. For instance the output range of the Figure 7 swings from $-200V_{dc}$ to $+200V_{dc}$ with five levels. If the straight forward fundamental frequency modulation technique is chosen it can be shown that, the charge and discharge of the cells in different levels will not be equal which results in capacitor voltage unbalance or unequal loading of input sources. It is possible to utilize CMCs without input sources as a reactive power compensator. But, if the output load in a CMC is resistive, these capacitors should be connected to isolated DC sources to supply the real power (Abu Tariq, 2006; SR

Bhatt, 2006; Dhana Prasad Duggapu, 2012; Ahmad Faiz Minai, 2011).

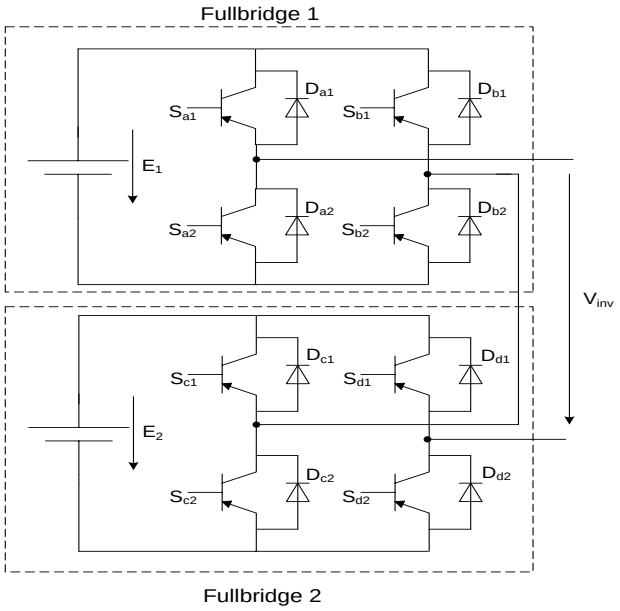


Figure 4(a): Cascaded five level inverter

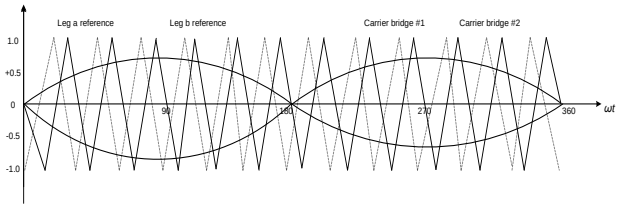


Figure: 4(b) Phase shifted modulation strategy and the associated outputs.

5. Simulink Model and Its Results

Simulink model of a five level multi inverter is given below

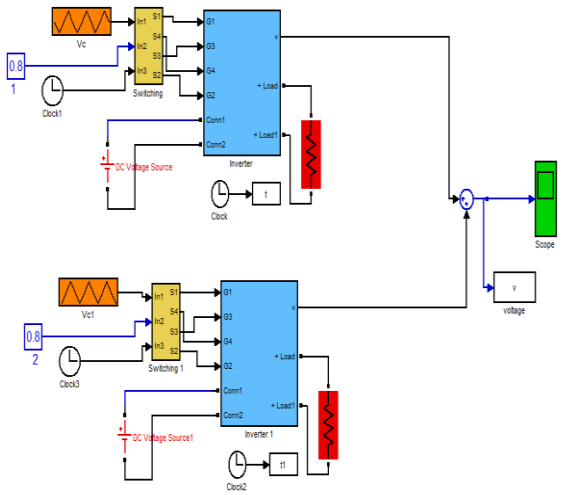


Figure 5(a): Simulink model of a Cascaded five level inverter

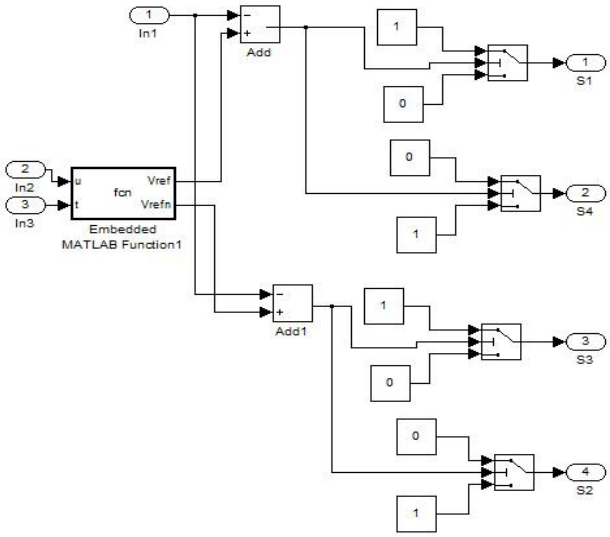


Figure 5(b): Simulink model of a switching block

In unipolar switching scheme, the switch pairs S_1S_2 and S_3S_4 of the full-bridge inverter of fig. 5(b) are not operated as pair. Instead, the switches of the first leg, i.e. S_1 and S_4, are operated by comparing the triangular carrier wave (V_c) with the sinusoidal reference signal (V_{ref}). The switches of the other leg, i.e. S_2 and S_3, are operated by comparing V_c with $-V_{ref}$. Following logic is used to operate these switches: (Muhammed H. Rashid, 2005; Zhong Du, 2009; L. M. Tolbert, 1997)

1. If $V_{ref} > V_c$, S1 is on and if $V_{ref} < V_c$, S_4 is on.
2. If $-V_{ref} > V_c$, S_3 is on and if $-V_{ref} < V_c$, S_2 is on.

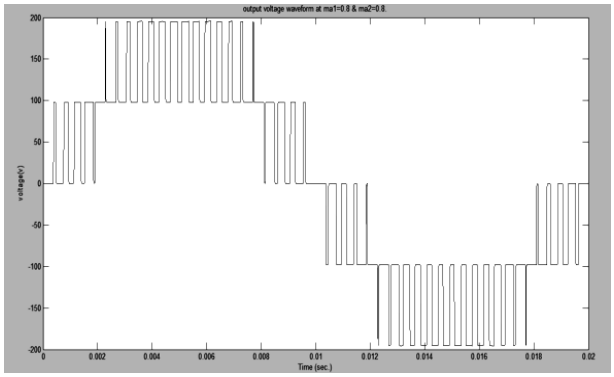


Figure 6: output voltage waveform at m_{a1}=0.8 & m_{a2}=0.8.

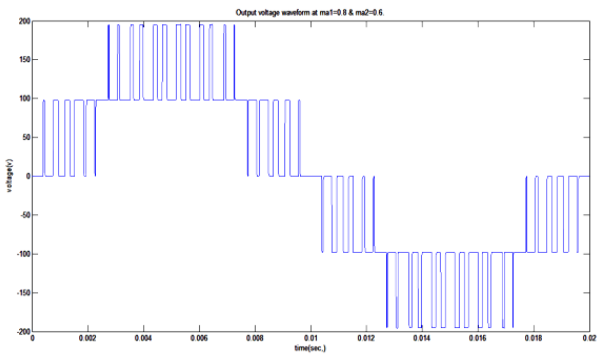


Figure 7: output voltage waveform at m_{a1}=0.8 & m_{a2}=0.6

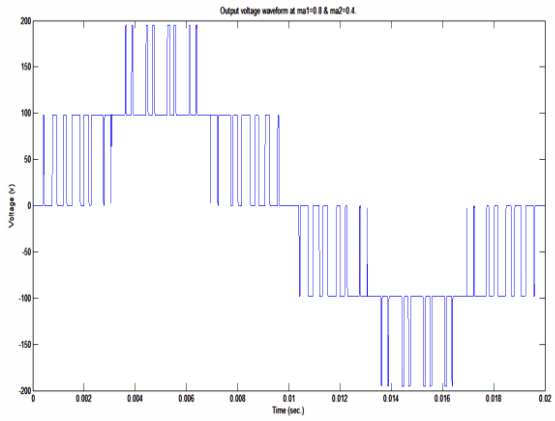


Figure 8: output voltage waveform at m_{a1}=0.8 & m_{a2}=0.4

Through different combinations of the four switches of both cells, both converter levels can Generate three different voltage outputs, +Vdc, 0, -Vdc. The number of output phase voltage levels is '5' because we use two photovoltaic sources. For instance the output range of the fig. 7 swings from -200V to +200V with five levels. In above figure output voltage waveforms for various value of different modulation index (ma) are shown. The pulse width of voltage waveform decreases by decreasing the value of modulation index (ma_2) and have constant modulation index (ma_1) (Muhammed H. Rashid, 2005; Fang Z. Peng, 2001; Leon M. Tolbert, 2005).

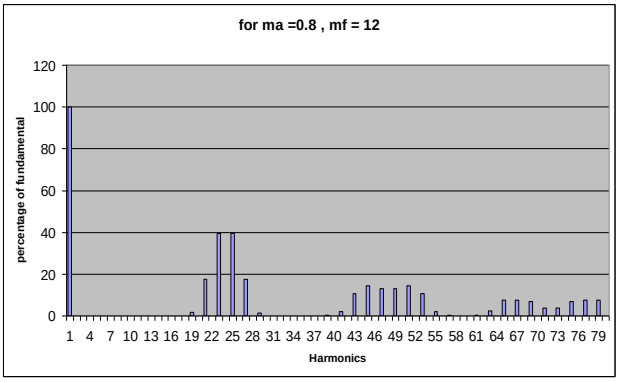


Figure 9: Harmonic spectrum of SPWM inverter with unipolar switching.

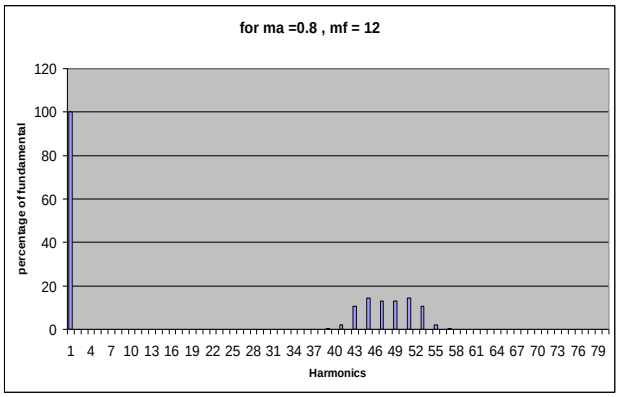


Figure 10: Harmonic spectrum of Multi-Level SPWM inverter with unipolar switching.

6. Generalized Harmonics Table for Five Level Inverter

The harmonics in the PWM inverter output voltage waveform appear as sidebands, clustered around the switching frequency and its multi ples, i.e. *mf*, 2*mf*, 3*mf* etc. This general pattern is true for all values of m_a in the range 0 through 1.0. Table 2(a) & 2(b) attempts to generalize the harmonic amplitudes with respect to the fundamental voltage for a five-level inverter. The table is created using the Simulink model (Ahmad Faiz Minai, 2011).

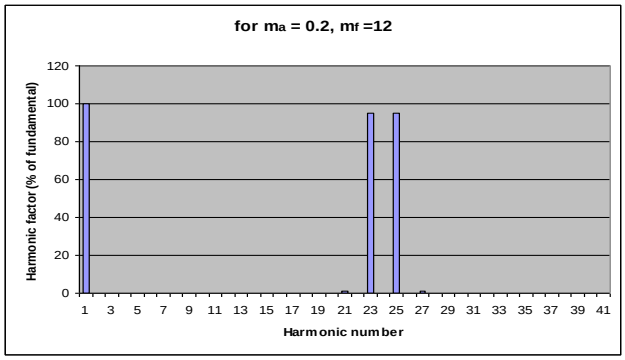
The amplitude of sidebands harmonic in multilevel inverter output voltage waveform is somewhat larger when the inverter is switching at low frequency. It can be observed that the amplitude of the fundamental component in the output voltage varies linearly with m_a.

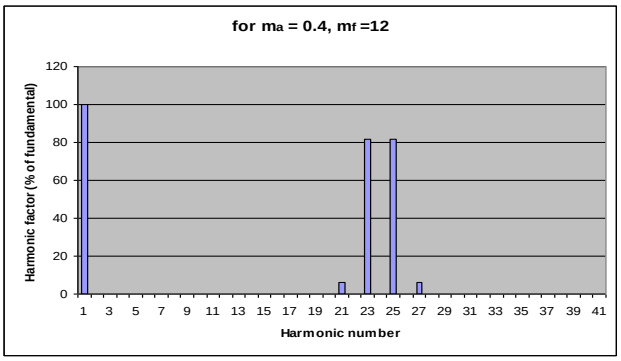
Table 2 (a): for two level inverter

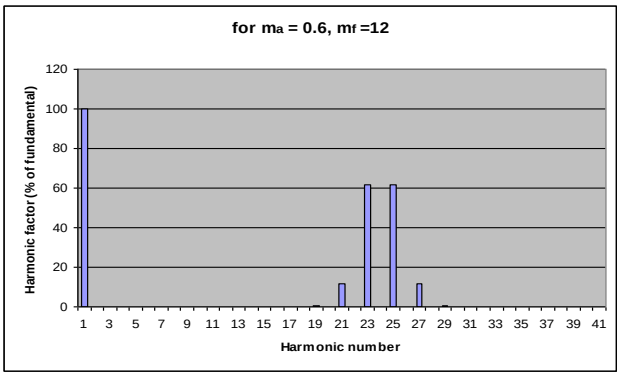
Harmonic number	m_a = 0.2	m_a = 0.4	m_a = 0.6	m_a = 0.8	m_a =1.0
$m_f \pm 1$	0.0004	0.0003	0.0004	0.0004	0.0288
$m_f \pm 3$	0.0013	0.0014	0.0013	0.0014	0.0284
$m_f \pm 5$	0.0025	0.0025	0.0025	0.0024	0.0310
$2m_f \pm 1$	3.4640	5.9600	6.7790	5.7670	3.3050
$2m_f \pm 3$	0.0500	0.4263	1.2850	2.5440	3.8950
$2m_f \pm 5$	0.0042	0.0041	0.0568	0.2267	0.5886
$3m_f \pm 1$	0.0005	0.0004	0.0004	0.0003	0.0141
$3m_f \pm 3$	0.0014	0.0015	0.0014	0.0013	0.0146

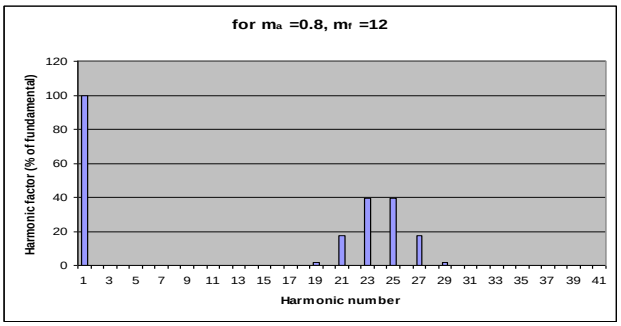
Table 2 (b): for multilevel inverter

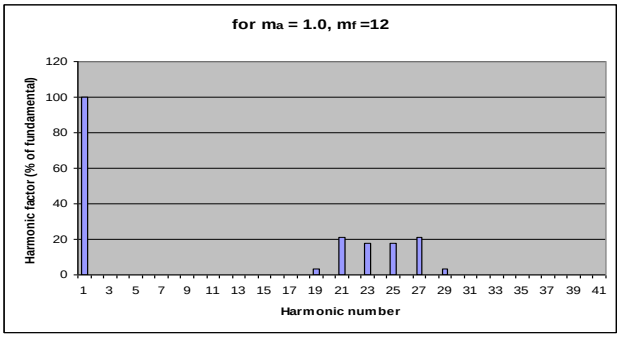
Harmonic number	m_a = 0.2	m_a = 0.4	m_a = 0.6	m_a = 0.8	m_a = 1.0
$m_f \pm 1$	0.0038	0.0037	0.0037	0.0039	0.0305
$m_f \pm 3$	0.0050	0.0050	0.0049	0.0051	0.0285
$m_f \pm 5$	0.0068	0.0068	0.0068	0.0067	0.0366
$2m_f \pm 1$	0.0003	0.0002	0.0002	0.0001	0.0266
$2m_f \pm 3$	0.0007	0.0006	0.0006	0.0007	0.0131
$2m_f \pm 5$	0.0011	0.0011	0.0011	0.0011	0.0119
$3m_f \pm 1$	0.0028	0.0030	0.0032	0.0034	0.0140
$3m_f \pm 3$	0.0022	0.0022	0.0024	0.0026	0.0130
$3m_f \pm 5$	0.0017	0.0017	0.0018	0.0018	0.0140

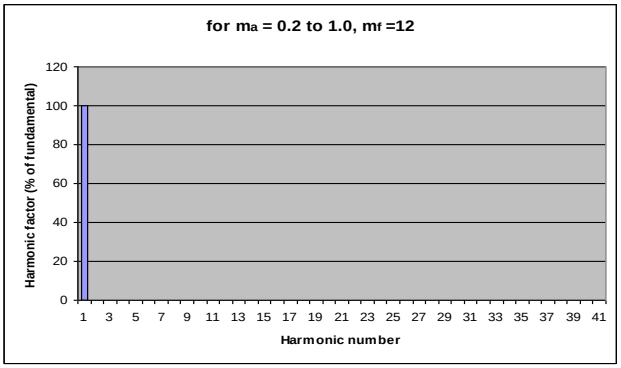












7. Total Harmonic Distortion (THD)

Total Harmonic Distortion (THD) is the most common power quality index to describe the quality of power electronic converter (I. Altas, 2007; Jose Rodriguez, 2002). In general, all the output voltage of power electronic converters is not purely sinusoidal. The THD of the output voltage can be defined as:

$$THD = \frac{\sqrt{\sum_{n=2,3...}^{\infty} V_n^2}}{V_1} = \frac{\sqrt{V_{rms}^2 - V_1^2}}{V_1}$$

Where n denotes the harmonic order and 1 is the fundamental quantity. For inverter application, THD represents how close the ac output waveform with pure sinusoidal waveform. A high-quality inverter system should have low THD.

Figure 11 shows the comparison of the THD between a five-level single-phase Inverter and a conventional two-level inverter configuration. The figure shows that for both cases, a poor THD are obtained when the inverter operated at low modulation index (Ahmad Faiz Minai, 2011).

A better THD is obtained when the inverter operated at higher modulation index. For example, at modulation index equals 1.0, it was found that THD for a MSMI inverter is three times better compared to a conventional two-level inverter (Jose Rodriguez, 2002).

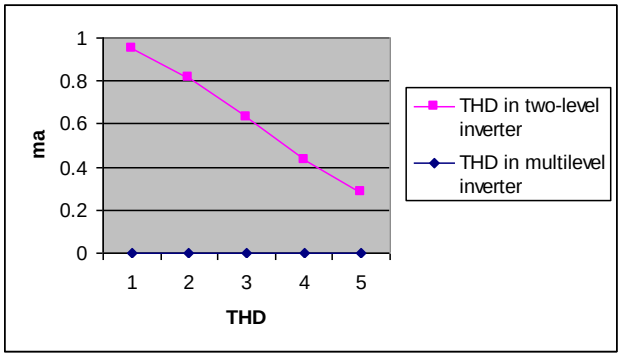


Figure 11: Comparison of the THD between a five-level single-phase Inverter and a conventional two-level inverter configuration.

8. Weight and Cost Comparison

Weight comparison is done for each topology by calculating the weight of all of the components of the inverters. The same switch is considered for all of the topologies to have a more accurate comparison. The IGBT FD300R06KE3 is used for all of the topologies. In the 5-level diode clamped multilevel inverter, the 5-level flying capacitor, the 5-level cascaded H- bridge and the two-level inverter, the capacitor C4DEFPQ6380A8TK is used, since the DC input voltages are higher, so a capacitor with higher voltage tolerance is needed. In the 9-level diode clamped multilevel inverter, the 9-level flying capacitor multilevel inverter and the 9- level cascaded H-bridge multilevel inverter the capacitor FFV34E0107K is used, since the DC input voltages are lower, so a capacitor with

lower voltage tolerance is needed. Table 3 shows the total weight and the total cost of all types of inverters (Mohammadreza Derakhshanfar, 2010).

Table 3: Weight and cost comparison for all types of inverters.

Type of inverter	Number of switches	Number of capacitors	Number of diodes	Weight (Kg)	Cost(€)
2-level	12	3	0	5.3	1861.2
5-level diode clamped	24	12	36	13.8	4493.3
5-level capacitor clamped	24	30	0	20.73	5894.2
5-level cascaded	24	6	0	10.67	3722.5
9-level diode clamped	48	24	72	19.704	7415
9-level capacitor clamped	48	60	0	21.72	7859.6
9-level cascaded	48	12	0	17.4	6659.2

Source: Chalmers

Conclusion

The choice of topology for each inverter should be based on what is the usage of the inverter. Each topology has some advantages and disadvantages. By increasing the number of levels, the THD will be decreased but on the other hand cost and weight will be increased as well. Also since the switching angles for switches are not the same, the drive circuit for each switch is separate from other switches. The two-level inverter has the lowest cost and weight in comparison with the other topologies. But this inverter has a very high THD; its THD is about 40% when one switching event for fundamental period is used. In weight and cost calculations, the price and weight of the filter should be considered, since it is not practical to have an output voltage with 40% THD. The cost and the weight of the 5-level multilevel inverters seem better than the 9-level multilevel inverters. By increasing the number of levels, the cost and weight of the multilevel inverter will be increased. The advantage that the 9-level multilevel inverters have over the 5-level multilevel inverters is their THD before filters, thus a filter will be needed. The 9-level multilevel inverters have lower THD than the 5-level multilevel inverters. For example the THD in the 5-level multilevel inverters and the 9-level inverters are 15% and 7%. It seems that using the 5-level inverter and a filter is a better design.

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