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Research Article

Fabrication of Nanostructure CdS Thin Film on Nanocrystalline Porous Silicon

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Abstract

In this work nanostructure CdS thin film with thickness 100 nm has been deposited successfully by flash evaporation technique (FET) on glass substrates at room temperature under vacuum of 10^{-5} mbar. XRD patterns of nanostructure CdS thin film was polycrystalline with a hexagonal structure and the preferred orientation is (002) with 2θ value about 26.25°. The value of average grain size is about 9.603 nm. The morphological properties of CdS thin film have been studied by AFM. The optical measurements indicated that CdS thin film has direct optical energy gap (E_g^{opt}) is about 4.18 eV. Nanocrystalline porous silicon (nPS) layers have been prepared during this work via electrochemical (EC) etching process of p-type silicon wafers at different etching times (10, 20 and 30) min. The morphological properties of the prepared nPS layers are studied. The Nanostructure CdS film was deposited on the porous silicon layers; this is achieved for preparation Nano-CdS/PS heterojunction solar cell. The electrical properties of prepared heterojunction have been studied in this work, that is represented by capacitance-voltage and current-voltage characteristics (under dark and illumination) characteristics for different etching times for nPS layer (10, 20 and 30 min) at room temperature.

Keywords: *Nanostructure CdS; Nanocrystalline porous silicon (nPS); Quantum dots; Flash evaporation technique (FET); Electrochemical etching process (EC).*

1. Introduction

The II–VI semiconductor nanocrystals exhibit interesting properties and their emission spectra is very narrow (spectrally pure) and the emission colour is simply tuned by changing their size. As the nanocrystal size decreases, the energy of the first excited state decreases qualitatively following a particle-in-a-box behaviour. This size dependence and the emergence of a discrete electronic structure from a continuum of levels in the valence and conduction bands of the bulk semiconductor result from quantum confinement; hence, semiconductor nanocrystals are referred to as quantum dots (Kippeny et al, 2002).. CdS with hexagonal structure is highly favorable for solar cell application as a window layer because of its suitable band gap and stability. CdS is one of the important materials for application in electro-optic devices, such as laser materials, transducers, photoconducting cells, photosensors, optical wave-guides and non-linear integrated optical devices (Senthil K. et al, 2001).

They can be deposited by different deposition techniques, such as sputtering (Lee J. H et al, 2007), molecular beam epitaxy **(**Brunthaler G et al, 1994**)**, chemical bath deposition (Moualkiaet H al, 2009), spray pyrolysis **(**Mathew **S** et al, 1995), thermal evaporation (Sathyamoorthyet R al, 2006), flash evaporation (Murali K. R et al, 2008), pulsed laser deposition (Tong X. L et al, 2008), and dip coating technique (Kaushik D et al, 2007). Comparing with some sophisticated techniques, vacuum thermal evaporation is very simple and inexpensive method, which can be used for large area thin film deposition. The problem associated with this technique is maintaining the stoichiometry in the deposition of materials composed of elements having different vapor pressures such as Cd and S in CdS. Hence flash evaporation technique (FET) has been used by many researchers to overcome the said problem (Murali K. R et al, 2008; Shah N. M et al, 2009).

Porous silicon has attracted great attention due to its room temperature photoluminescence in the visible light range (Canham L. T, 1990). As we know that, the bulk crystalline silicon has an indirect gap at 1.1 eV at room temperature, which results in a very inefficient radiative recombination and produced light in the infrared region. Therefore, the strong visible light emission in porous silicon is quite surprising and such structure can exhibit a large variety of morphologies and particles sizes. Porous silicon shows different features in comparison to the bulk silicon such as shifting of fundamental absorption edge into the short wavelength and photoluminescence in the visible region of the spectrum. However, different hypothesis is reported on photoluminescence from porous silicon surface. The first includes the quantum confinement effect which is due to the charge carriers in narrow crystalline silicon wall separating the pore walls, the second is due to the presence of luminescent surface

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species trapped in the inner walls as the source light emission and the third one is due to the presence of surface confined molecular emitters (i.e. siloxene), (Pavesi L and Guardini R, 1996; Weng Y. M et al, 1993).

Porous silicon consists of a network of nanoscale sized silicon wires and voids which formed when crystalline silicon wafers are etched electrochemically in hydrofluoric acid based electrolyte solution under constant anodization conditions. The precise control of porosity and thickness allows the tailoring of optical properties of porous silicon and has opened the door to a multitude of applications in optoelectronics technology. Such structures consist of silicon particles in several nanometer size separated by voids. Hence, porous silicon layers are regarded as nanomaterials, which can be obtained by the electrochemical etching of silicon wafer. Porous silicon structures has good mechanical robustness, chemical stability and compatibility with existing silicon technology therefore has a wide area of potential applications such as waveguides, 1D photonic crystals, chemical sensors, biological sensors, photovoltaic devices etc. (Agrawal V. and del Rio J. A, 2003; Oton C. J et al, 2003).

Photovoltaic is a renewable energy, which is helpful to reduce the pollution and climate change effects. Today, photovoltaic industry is dominated by silicon solar cells technology because of the reduced cost. Due to wide use of solar energy, there is the need of creation of new technologies and materials hence; porous silicon is expected to be promising one. The crystalline silicon is an important and dominant material over several years due to its well-known properties and established infrastructure for photovoltaic manufacturing (Green M. A, 2007). It is the basic material for the production of solar cell and about 90% of fabricated solar modules are made of crystalline silicon. Presently, an increasing interest has been shown in antireflection coating made from porous silicon by researcher (Boeringer D. W and Raphael Tsu, 1994; Hajji M et al, 2005). For solar cell, porous silicon layer acts as an ultra efficient anti-reflection coating, while a graded layer with varying expanded band gap offers increased absorption in visible spectrum regions.

The objective of this work is to the preparation of the nanostructure CdS thin films using Flash Evaporation technique (FET), and discuss the structural properties, surface morphology and optical properties of the prepared thin film and to use CdS as a transmittance layer in solar cell. In section two, the synthesis and characterization of electrochemically anodized nanocrystalline porous silicon layers is done, then, the setup was used in fabrication as a device of Nano-CdS/PS heterojunction solar cell, and investigating the electrical properties of the heterojunction.

2. Experimental

2.1. Nanostructure CdS thin film preparation

Nanostructure CdS thin film was fabricated onto cleaned glass substrates with thickness 100 nm by flash evaporation technique. Cleaning of substrate is important in fabrication of thin films, because it greatly influences the properties of the films deposited on it and has strong effect on the adhesion properties of the deposited films. The glass substrates were cleaned using soap-free detergent and followed by multiple rinsing in boiling water then rinsing in distilled water to remove traces of detergent, and then the substrates were cleaned in an ultrasonic for 10 min with ethanol. The last step of clean was drying the substrates by blowing air.

The evaporation of CdS thin film was done by using vacuum system model (Edward 306A). CdS Powder of 99.99% purity was evaporated from a molybdenum boat. The powder is dropped into a heated boat from the feed through passing through a guide funnel by manual vibrating handmade system. The boat heated up to the temperature about 1750 K appropriate to evaporate the CdS powder at pressure of 10^{-5} Torr at ambient temperature in vacuum chamber, the deposition rate was about 1.2 nm/s.

2.2. Nanocrystalline porous silicon layers preparation

Crystalline silicon (C-Si) wafers (thickness 500 μm and resistivity 1.5 Ω.cm) in (400) orientation used to prepare nPS by using the Electrochemical etching process. The silicon is cleaned to remove any contamination on the surface. These pieces were rinsed with ethanol to remove dirt, followed by etching in dilute Hydrofluoric acid (10% HF) for 10 min to remove the native oxide layer. The samples rinsed with ethanol and left in environment for a few minutes to dry.

The porous silicon samples were prepared by electrochemical anodic dissolution of doped p-type silicon substrates in hydroflounce acid and ethanol with platinum electrode as cathode. The electrolyte was prepared by mixing HF with concentration (39%) and ethanol (C_2H_5OH) in 1:1ratios. The porous layers on the surface of these samples were prepared at current densities of 50 mA/cm^2 with various etching times (10, 20 and 30) min.

2.3. Nano-CdS/PS heterojunction solar cell preparation

After preparing the nPS samples by using the Electrochemical etching process, the Nanostructure CdS thin films with thickness 100 nm were deposited on the porous silicon layers; this is achieved by using Flash evaporation technique for preparation Nano-CdS/PS heterojunction.

2.4. Characterization techniques

The crystallographic structure of films was analyzed with x-ray diffractometer (Model XRD-6000, Shimadzu, Japan) using Cu-K_α (λ=1.54Å) radiation. Diffraction patterns have been recorded over the 2θ range of 20^o to 60^o at the scan rate of 10^o min^{-1}.

The surface morphology and roughness of prepared samples were obtained by atomic force microscopy (Scanning probe Microscope type AA3000), supplied by Angstrom Advanced Inc. in non-contact mode. The transmission spectrums of Nanostructure CdS thin film was obtained using UV-Visible recorder spectrophotometer (Type Shimadzu- Japan), Model (UV-

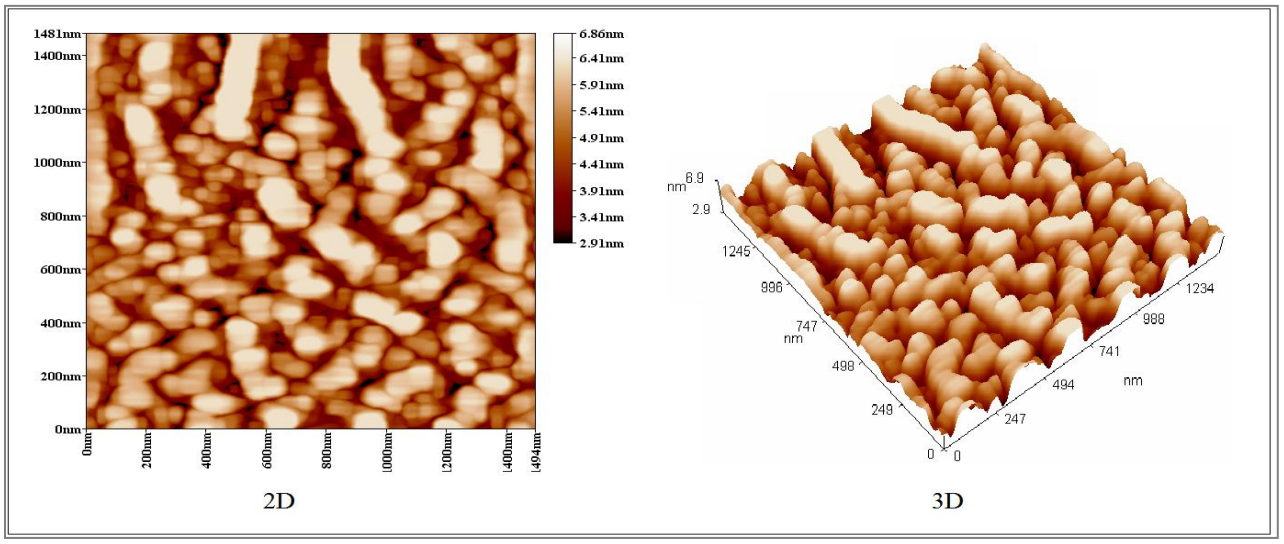

Fig. 2 2D and 3D AFM images of Nanostructure CdS thin film

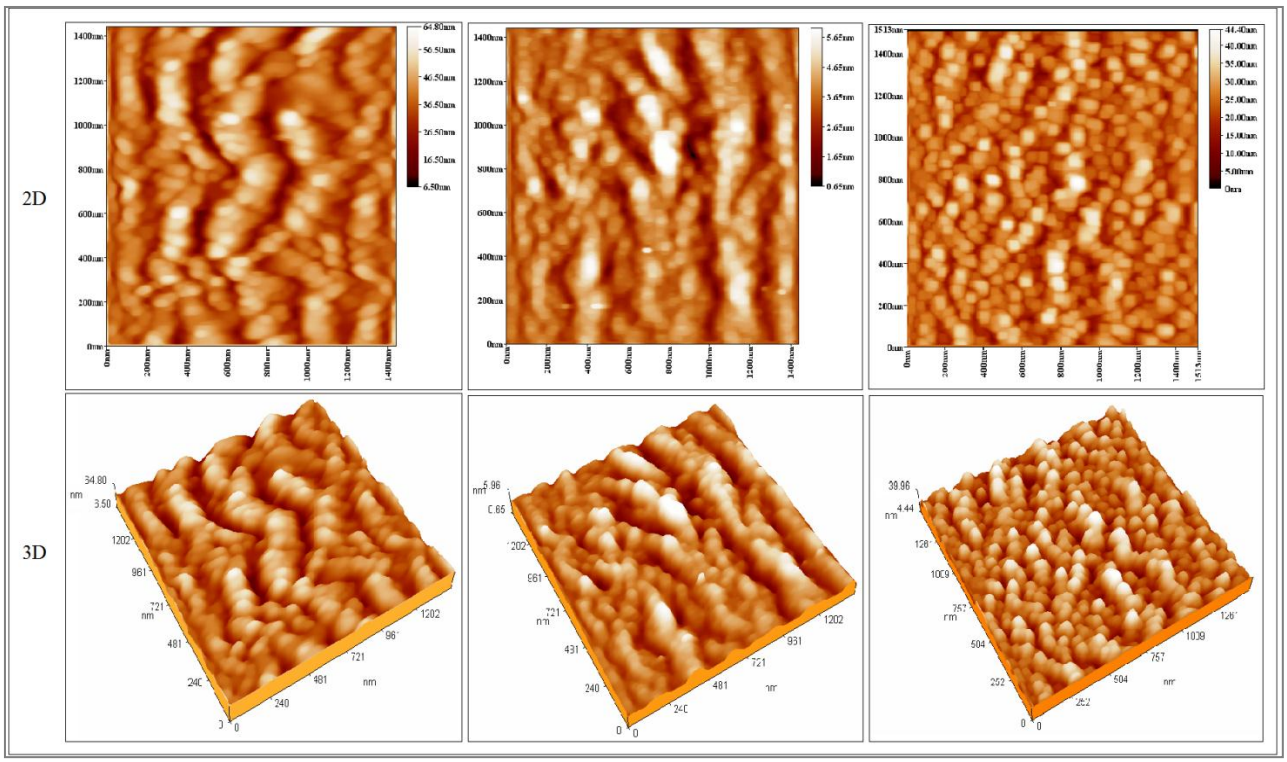

Fig. 3 2D and 3D AFM images of the as-anodized Nanocrystalline porous silicon surface structure formed on p-type (400), prepared with etching time of a) t= 10 min with porous average diameter (63.76 nm), b) t= 20 min with porous average diameter (59.30 nm), c) t= 30 min with porous average diameter (53.18 nm), at HF concentration 39% and current density of 50 mA/cm^2

160) in the wavelength range (200-1100) nm. The electrical measurements for Nano-CdS/PS heterojunction, which was prepared at constant substrate temperature with different etching times of nPS layers includes current-voltage characteristic measurements in the dark and under illumination conditions by using HP-R2C unit model 4274A and 4275A multi-frequency LRC meter as well as capacitance-voltage characteristic measurements by using Keithley Digital Electrometer 616, voltmeter and D.C. power supply.

3. Results and discussion

3.1. Structural properties

Figure 1 shows the x-ray diffraction patterns of the CdS thin film prepared by flash evaporation technique on a glass substrate at room temperature. The x-ray diffraction patterns of the sample exhibit small peaks at 26.52° corresponding to the (002) directions. This peak corresponds to the hexagonal phase. The lattice parameter

values a, and c have been calculated and are a = 4.106 Å and c = 6.637 Å which are in agreement with the JCPDS data (80-006), (JCPDS, 2000).

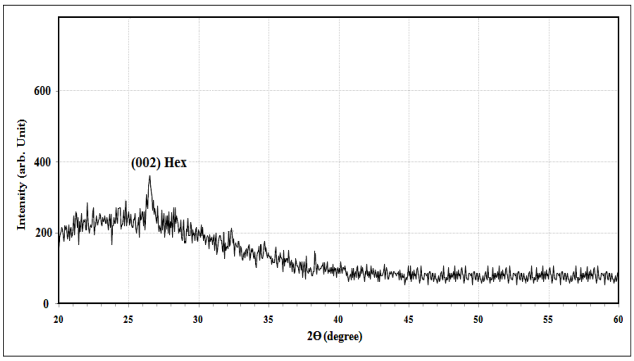

Fig. 1 XRD patterns of Nanostructure CdS thin film

The presence of small peaks in the x-ray diffractogram reveals the formation of nanocrystalline CdS film. The peaks are not sharp indicating that the average crystallite size is small. Due to size effect, the peaks in the diffraction pattern broaden and their widths become large as the particles become smaller.
The average size of grains has been obtained from the x-ray diffraction pattern using the Debye-Scherrer's formula

$$GS=K\lambda/\beta\cos\theta \quad (1)$$

Where the constant K is a shape factor usually 0.94, λ the wavelength of X-ray (0.15418 nm), β the FWHM in radians and θ is the Bragg's angle. We use the standard (0 0 2) H reflection at 2θ = 26.52°.

The strain values ε can be evaluated using the following relation (Suthankissinger N. J. and Jayachandran M, 2007)

$$\varepsilon=\beta\cos\theta/4 \quad (2)$$

Table 1 summarizes the deposition of CdS nanostructures parameters on glass substrates.

Table 1 Comparison of structural parameters, the interplanar distance (d), FWHM, Grain size (GS) and Strain (ε) of the Nanostructure CdS thin film

2θ (Degree)	26.52
d Exp. (Å)	3.3579
d Std. (Å)	3.3572
hkl	002
FWHM (Degree)	0.85
Grain size (GS) (nm)	9.603
Strain (ε)*10^{-3}	3.608
phase	Hex CdS

3.2. Morphological analysis

Figure 2 shows the AFM image of flash evaporation CdS thin film. The image shows well defined particle like features with granular morphology and indicates the presence of small crystalline grains.

The root mean square (RMS) surface roughness of the film is 0.91 nm. The image also reveals that the film is homogeneous without any cracks and is continuous with very well connected grains. The surface roughness is unavoidable due to the three-dimensional growth of the films. Table 2 shows the value of average roughness and average diameter.

Table 2 The value of average roughness, RMS and average Diameter

Average roughness (nm)	RMS (nm)	Average Diameter (nm)
0.77	0.91	56.95

Figure 3 shows the AFM images of Nanocrystalline porous silicon (nPS) layers prepared by electrochemical etching (EC) process for different etching times (10, 20 and 30) min. It can be noticed from the Figure that the nanospikes size is reduced with increasing the etching time up to 30 minutes. Above this value, the nanospikes start too annihilated in height and distribution. Thus, the etching time is limited to 30 minutes for the material type in order to create reasonable nanospikes structure on the surface of the p-type silicon.

3.3. Optical properties

The optical transmission studies were carried out in the wavelength range 200 to 1100 nm. Figure 4 shows that film has high light transmission in the visible region, so CdS film, which deposited by flash evaporation of the same conditions can actively used as a window material in solar cells.

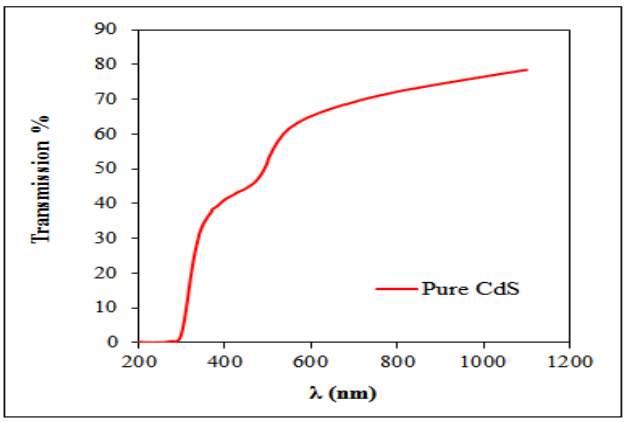

Fig. 4 Transmittance Spectra of Nanostructure CdS thin film

Figure 5 shows optical absorption spectra of CdS. Optical band gap is calculated using the Tauc relation (Tauc J, 1974):

$$(\alpha h\nu)^{1/n}=A(h\nu-E_g) \quad (3)$$

Where A is a constant and E_g is the band gap of the materials and exponent n depends on the type of transition. For direct allowed transition n=1/2. To determine the

possible transitions, $(\alpha h\nu)^2$ versus hν is plotted and corresponding band gap were obtained from extrapolating the straight portion of the graph on hν axis. The direct band gap value of the sample has been obtained from $(\alpha h\nu)^2$ vs plot as shown in the Figure 6. The direct band gap value of the sample is found to be 4.18 eV, which is greater than the bulk band gap value of CdS (2.42 eV at 300 K), and this indicates the formation of nanoparticles. This value is shifted compared with the bulk value and this could be a consequence of a size quantization effect in the sample. The reduction in particle size gives a shift in the optical band gap of the sample. The obtained band gaps for CdS nanocrystals is the biggest value between all published values (Tong X. L et al, 2007; Khallaf H et al, 2008; Faraj M.G et al, 2011; El-Rabaie, S et al, 2014; Devi R et al, 2007), we suggest that this is due to the obtained crystallite size value for CdS nanocrystals in this work is the smallest value between all published values (Tong X. L et al, 2007; Khallaf H et al, 2008; Faraj M.G et al, 2011; El-Rabaie S et al, 2014; Devi R et al, 2007; Al-Jumaili Hamid S. and mahmood Taha N, 2013; Das Ruby and Pandey Suman, 2011).

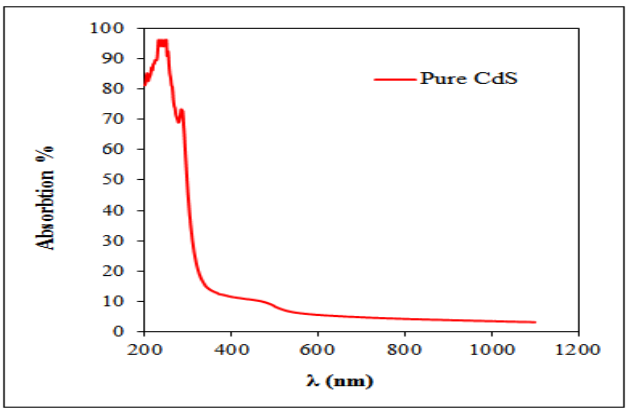

Fig. 5 UV-VIS absorption spectra of Nanostructure CdS thin film

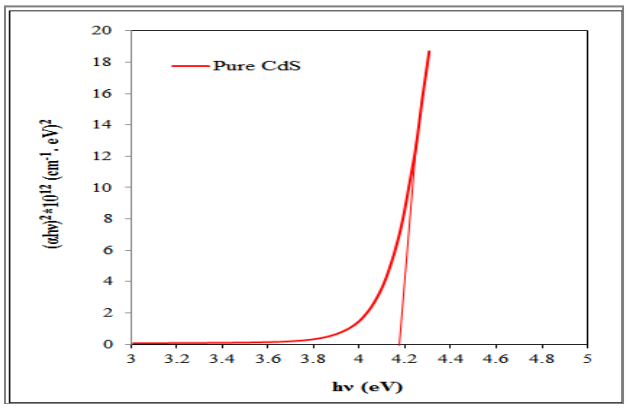

Fig. 6 A plot of $(\alpha h\nu)^2$ versus hν of Nanostructure CdS thin film

The enhancement of band gap is attributed to the quantum size effect of these small crystallites, although the diameters of the nanoparticles are quite larger than the excitonic Bohr radius (~3.5 nm) of CdS (Mondal S. P et al, 2007; Maity R. and Chattopadhyay K. K., 2006). Semiconductor nanoparticles (NPs) are expected to exhibit quantum confinement effects when their size becomes comparable to the Bohr exciton radius, which results in an increase in the energy gap relative to that of the bulk solid (Kayanuma Y, 1988).

3.4. Electrical Properties of Nano-CdS/PS heterojunction

3.4.1. Capacitance-Voltage Characteristic of Nano-CdS/PS heterojunction

The capacitance-voltage characteristics have been studied in this work. The variation of capacitance as a function of reverse bias voltage in the range of (0-1) V for Nano-CdS/PS heterojunction, which prepared at different etching times (10, 20 and 30) min are shown in Figure 7. It is observed from this figure that the capacitance decreases with increasing the reverse bias. This decreasing was non-linear, that the capacitance becomes constant approximately at high voltages. This behavior is attributed to the increasing in the depletion region width which leading to the increasing of built-in voltage (Thangaraju B and Kaliannan P, 2000); it is obvious from this Figure that the capacitance at zero bias voltage (C_o) decreases with the increasing of etching time of nPS layers (see Table 3). This is attributed to the increase of porosity with the increasing of etching time, which leads to the increasing of the depletion region width and decreasing the capacitance.

The relation between inverse capacitance squared (C^{-2}) against the reverse bias at different values of etching time are shown in Figure 8. A linear relationship between C^{-2} and reverse bias voltage was obtained for the structure, this linear relationship represents that the junction was abrupt type. The interception of the straight line with voltage axis at ($1/C^2 = 0$), represents the built-in voltage. According to the capacitance-voltage measurements, we can calculate the width of the depletion region by (Adams M. J. and Nussbaum A, 1997):

$$W = \varepsilon_s / C_o \quad (4)$$

Where C_o is the capacitance at zero biasing voltage, and

$$\varepsilon_s = (\varepsilon_n \varepsilon_p)/ (\varepsilon_n + \varepsilon_p) \quad (5)$$

Where ε_s is the semiconductor permittivity for the two semiconductor materials.

Table 3 Values of C_o, W and V_{bi} for Nano-CdS/PS heterojunction with different etching times of nPS layers

Thickness (nm)	Etch. Time (min)	C_o (nF)	V_{bi} (Volt)	W (μm)
100	10	0.700	0.41	0.0201
	20	0.548	0.49	0.0257
	30	0.416	0.53	0.0339

The values of capacitance (C_o), the built-in voltage (V_{bi}) and the width of the depletion layer (W) are shown in Table 3. Assuming that the resulting junction is one-sided

junction, these data were calculated according to Anderson model. Also, it is observed from this Table that the depletion width increases with the increasing etching time due to the decreasing in the carriers' concentration which leads to the decreasing of the capacitance.

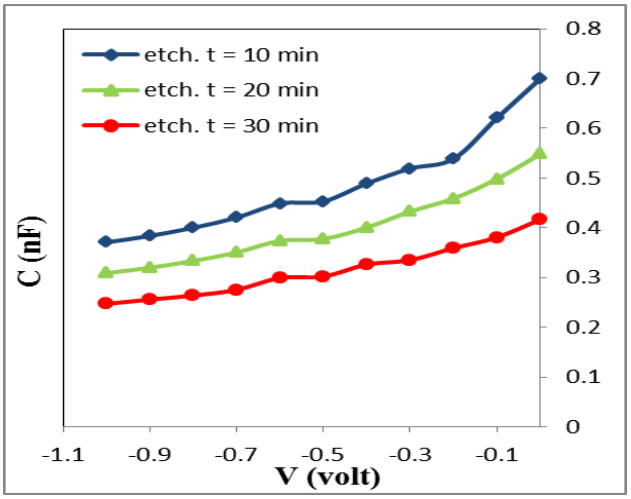

Fig. 7 The variation of capacitance as a function of reverse bias voltage for Nano-CdS/PS heterojunction with different etching times of nPS layers

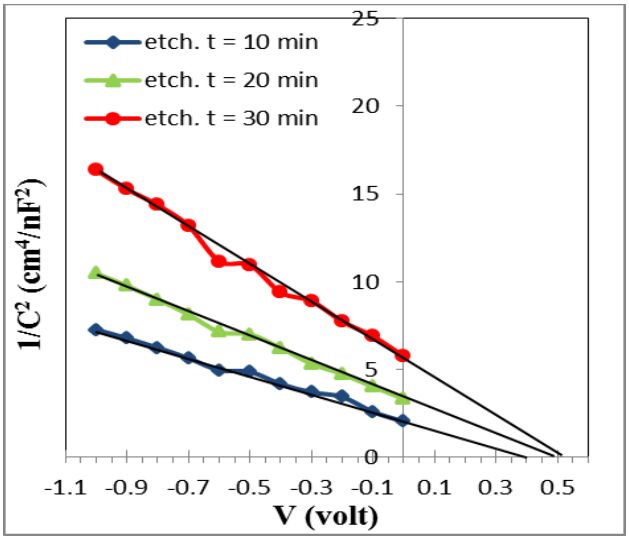

Fig. 8 The variation of $1/C^2$ as a function of reverse bias voltage for Nano-CdS/PS heterojunction with different etching times of nPS layers

3.4.2. Current-Voltage Characteristic of Nano-CdS/PS heterojunction

The current-voltage curves are the most commonly used characterization tool for the devices. In this technique, the current is measured as a function of voltage of the heterojunction, in both dark and light. Figure 9 shows the I-V characteristics for Nano-CdS/PS heterojunction at dark and reverse bias at room temperature, at different etching times (10, 20 and 30) min. In general, the forward dark current is generated due to the flow of majority carriers and the applied voltage inject majority carriers which leads to decrease the value of built-in potential, and decrease the width of the depletion layer. Then majority and minority carrier concentration is higher than the intrinsic carriers concentration (n_i < np) which leads to generate recombination current at the low voltage region because that the excitation electrons from V.B to C.B will recombine with the holes which found at the V.B, and this is observed by increasing in recombination current at low voltage region. While the tunneling current is observed at high voltage region after that, there is a fast exponential increase in the current magnitude with increasing the voltage and this is called diffusion current, which is dominated (Thangaraju B. and Kaliannan P, 2000). Also, the reverse bias current contains two regions in the voltage region the current increases with increasing the applied voltage, and the generation current dominates. At the high voltage region, the current is stabilizes and becomes independent of the bias potential; this is called the diffusion current (Aly N. I et al, 2001; Sankara N et al, 2005). In addition, the current-voltage characteristics exhibit rectification behavior may be due to the hetrojunction potential barrier at the CdS/PS interface **(**Canham L. T, 1997). The rectification factor indicates the ratio between forward and reverse current at a certain applied bias voltage.

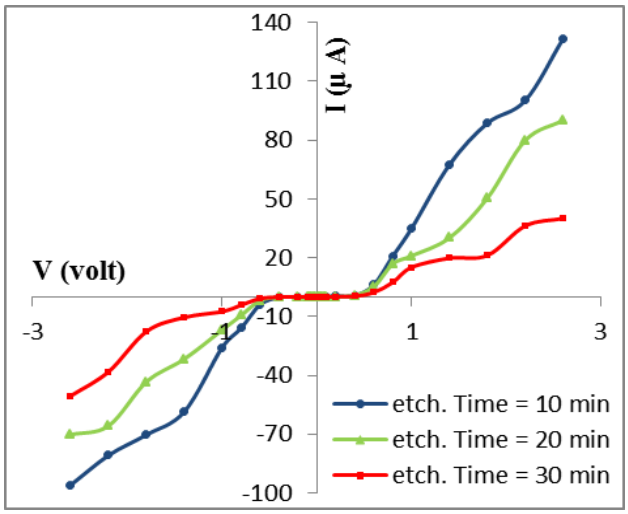

Fig. 9 I-V characteristics at dark for Nano-CdS/PS heterojunction at forward and reverse bias voltage with different etching times of nPS layers

This Figure illustrates that the current flow in the forward bias decreases with the increasing of etching time. Due to the high density of states of the nPS layer which will result in screening of internal field inside the nPS layer, this field would be nearly homogenously distributed through the nPS layer at higher voltages (V > 1 V), therefore, the forward bias characteristics will be controlled by the PSi layer resistance. This result explains the lowering of flow current in forward bias with the increasing of etching time of nPS layers, since the porosity of nPS layer increases with etching time and hence the resistance of nPS layer becomes too high which leads to low forward current. Figure 10 represents I-V characteristics under illumination with power intensities (69.19 mW/cm^2) at

room temperature of the Nano-CdS/PS heterojunction, containing nPS layers prepared at different etching times (10, 20 and 30) min. The photocurrent has been observed in reverse bias only, and we can see from this figure, that the presence of the light illumination strongly increases the reverse current. The photocurrent is always in the reverse bias direction due to it increases by increasing the depletion region width. The increasing of the reverse bias voltage leads to the increase in the internal electric field, which leads to an increasing in the probability of the separated electron-hole pairs.

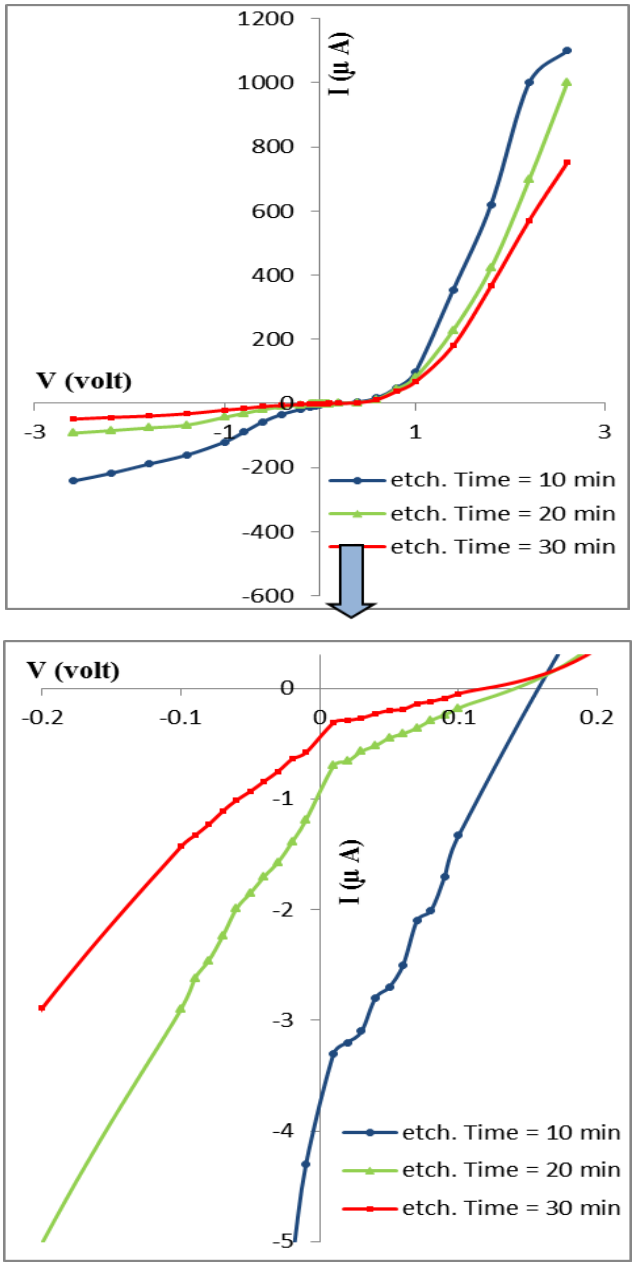

Fig. 10 I-V characteristics under illumination for Nano-CdS/PS heterojunction at forward and reverse bias voltage with different etching times of nPS layers

The effect of preparation conditions of nPS layer such as etching time has very important effect on the photocurrent characteristics of the device, where one can observe from Figure 10, that the photocurrent is reduced with the increasing of etching time. This result can be explained since the porosity of nPS layer increases with the increasing of etching time. The increasing of porosity leads to increase the resistivity of nPS layer; therefore, the photocurrent will decrease.

Conclusion

Nanostructure CdS thin film was fabricated by flash evaporation technique (FET). X-ray diffraction patterns exhibit small peaks with a hexagonal phase and the value of average grain size is about 9.603 nm. The optical transitions in nanostructure CdS film is direct transition and the value of optical energy gap is about 4.18 eV. The capacitance for Nano-CdS/PS Solar Cell decreases with the increase of the reverse bias voltage and with the increasing of etching time of nPS layers, the value of built-in potential for heterojunction increases with the increasing of etching time of PS layers. The current-voltage characteristics of the CdS/PS solar cell under dark conditions show that forward bias current variation approximately exponentially with voltage bias. This conforms to tunneling-recombination model, and reverse bias shows little stop and soft breakdown voltage, and the forward current decreases with the increasing of etching time. From the current-voltage characteristics under illumination, the photocurrent increases with the increasing of applied reverse bias voltage and it is reduced with the increasing of etching time.

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