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Research Article

A Comparative Analysis of Tunneling FET Characteristics for Low Power Digital Circuits

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Abstract

The technology used in today's transistors is called "field effect" whereby voltage induces an electron channel that activates the transistor. But field effect technology is approaching its limits, particularly in terms of power consumption. With the rapid increase of the number of circuits on a chip, power consumption has increased and appeared as the leading design challenge. In order to achieve significantly reduced power consumption, the transistor operating voltage needs to be reduced. However; the reduction in power consumption of the MOSFETs used in today's electronic circuits is reaching the fundamental limit. However, the reduction in power consumption of the MOSFETs used in today's electronic circuits is reaching the fundamental limit. This review introduces and summarizes progress in the development of the tunnel field-effect transistors (TFETs) including its origin, current experimental and theoretical performance relative to the metal–oxide–semiconductor field-effect transistor (MOSFET), design tradeoffs, and fundamental challenges.

Keywords: *TFETs, subthreshold swing, band to band tunneling, I_{ON}/I_{OFF} ratio.*

1. Introduction

CMOS technology has been an ideal framework to realize digital designs due to its desirable performance, power, cost and reliability characteristics. However as these devices are scaled down to feature sizes in the order of atomic dimensions, fundamental limits are approached causing transistors and wires to behave in a manner that is far from ideal. In scaling all of device dimensions along with supply voltages are reduced by the same factor. By scaling the MOSFET, speed of the circuit increases, area occupied and power consumed by the circuit decreases. Hence the power density of the circuit remains unchanged. In recent years scaling of voltage is limited due to difficulty in maintaining performance of circuit. So there is a tradeoff between transistor density and performance to mitigate the power density. Apart from voltage scaling, MOSFET suffers from short channel effects (SCEs) like drain induced barrier lowering (DIBL), punch through, quantum tunneling through gate, impact ionization etc., all these phenomena degrades the performance of circuit. Switching characteristics of MOSFET also degraded because of increase in leakage current. Alternative devices are investigated to replace the MOSFETs because of their scaling problems.

In particular, there is a focus on devices which act as field-effect transistors (FETs), where a change of gate voltage turns the current ON and OFF, but which use band-to-band tunneling in their ON-state, as well as in the transition between the OFF- and ON-states . These devices have the potential for extremely low OFF-current, and present the possibility to lower the subthreshold swing beyond the 60-mV/dec limit of conventional MOSFETs. One such interesting device is the Tunneling FET (TFET) which utilizes the band-to-band tunneling as the conduction mechanism have emerged as one of the most promising candidates for ultra-low voltage/power operation.TFETs do not suffer from severe SCEs. Switching characteristics of TFET are good because of high ION/IOFF ratio and steeper subthreshold swing.In the past, the tunnel effect was known to disrupt the operation of transistors. According to quantum theory, some electrons cross the barrier, even if they apparently don't have enough energy to do so. By reducing the width of this barrier, it becomes possible to amplify and take advantage of the quantum effect – the energy needed for the electrons to cross the barrier is drastically reduced, as is power consumption in standby mode. By replacing the principle of the conventional field effect transistor by the tunnel effect, one can reduce the voltage of transistors from 1 volt to 0.2 volts. In practical terms, this decrease in electrical tension will reduce power consumption by up to a factor of 100.

The power consumption becomes a major bottleneck for further scaling. The continued reduction of MOSFET size is leading to increased leakage current due to short channel effects. A promising alternative for MOSFET which does not suffer from these limitations is Tunneling FET.

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CMOS devices rely on a switching mechanism based on the modulation of thermionic emission from a thermally broadened Fermi function and are thus bound to a minimum inverse subthreshold swing of 60mV/dec at room temperature. This is a major obstacle for a further reduction of the operational voltage and hence the power consumption of integrated circuits. An alternative nano-device structure is the Tunnel-FET (TFET), this paper explains the structure of a Tunnel FET and how it functions and discusses subthreshold slope for both MOSFETs and Tunnel FETs.

2. TFET structure and characteristics

Scaling the supply voltage provides a quadratic reduction in switching energy. However, Supply voltage scaling in MOSFET designs reaches a plateau due to the concerns of increased static energy consumption. This is because the threshold voltage (Vt) of the MOSFET must also be scaled along with the supply voltage in order to maintain a sufficiently high on-state drive current (ION) and thereby avoid performance degradation. This reduction of the threshold voltage (Vt), however, results in an exponential increase of the off-state leakage current (IOFF) which in turn increases static energy consumption. Thus, there is a fundamental limit to the scaling of MOSFET threshold voltages and, consequently, the supply voltage. This limit is determined by the sub-threshold slope of MOSFETs and overcoming this limit provides the primary motivation for research into alternative technologies.

2.1 TFET device and structure

In contrast to MOSFETs, in which charge carriers are thermally injected over a barrier, the primary injection mechanism in a TFET is interband tunneling, whereby charge carriers transfer from one energy band into another at a heavily doped p+–n+ junction. This tunneling mechanism was first identified by Zener14 in 1934. In a TFET, interband tunneling can be switched on and off abruptly by controlling the band bending in the channel region by means of the gate bias. Structure of n-type and p-type TFET with n-type and p-type MOSFET is shown in fig 1.

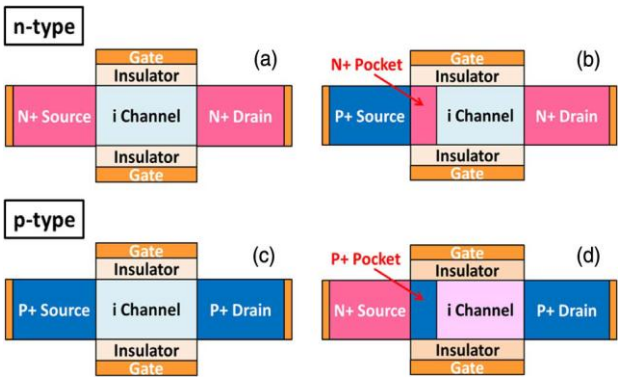

Figure 1 Structures of the (a) n-type MOSFET (b) n-type p-n-p-n TFET (c) p-type MOSFET and (d) p-type p-n-p-n TFET.

This function can be realized in a reverse-biased p-i-n structure (Fig. 2a). In principle, the TFET is an ambipolar device, showing p-type behavior with dominant hole conduction and n-type behavior with dominant electron conduction. In the TFET off state (dashed blue line in Fig. 2b), the valence band edge of the channel is located below the conduction band edge of the source, so BTBT is suppressed, leading to very small TFET off-state currents that are dictated by the reverse-biased p-i-n diode. Applying a negative gate voltage (solid red curve in Fig. 2b) pulls the energy bands up. A conductive channel opens as soon as the channel valence band has been lifted above the source conduction band because carriers can now tunnel into empty states of the channel. Because only carriers in the energy window $\Delta\Phi$ can tunnel into the channel, the energy distribution of carriers from the source is limited; the high-energy part of the source Fermi distribution is effectively cut off, as shown in Fig. 2b. Thus the electronic system is effectively 'cooled down', acting as a conventional MOSFET at a lower temperature.

This filtering function makes it possible to achieve an *S* of below 60 mV per decade (Fig. 2c). However, the channel valence band can be lifted by a small change in gate voltage, and the tunneling width can effectively be reduced by the gate voltage. As a consequence of the BTBT mechanism, *S* in a TFET is not constant, but depends on the applied gate–source bias, as indicated in Fig. 2c, increasing with the gate-to-source bias. The key to the better voltage scaling of a TFET than a MOSFET is that *S* remains below 60 mV per decade over several orders of magnitude of drain current.

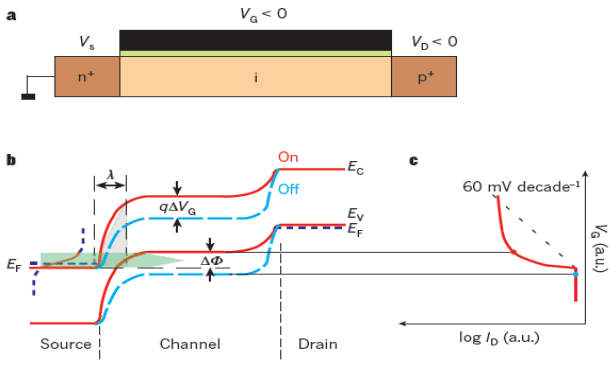

Figure 2 Principle of operation of a TFET.(a), Schematic cross-section of p-type TFET with applied source (*VS*), gate (*VG*) and drain (*VD*) voltages.(b) Schematic energy band profile for the off state (dashed blue lines) and the on state (red lines) in a p-type TFET. **c.** Schematic transfer characteristics.

Tunnel FETs are capable of achieving a sub-60mV/decade subthreshold slope and are resilient to short channel effects. These characteristics provide an opportunity to scale the supply voltage without significantly impacting the circuit delay or leakage component of energy consumption. Further, the leakage current (I_{OFF}) of TFETs is far lower than MOSFETs, increasing its attractiveness for energy constrained designs.

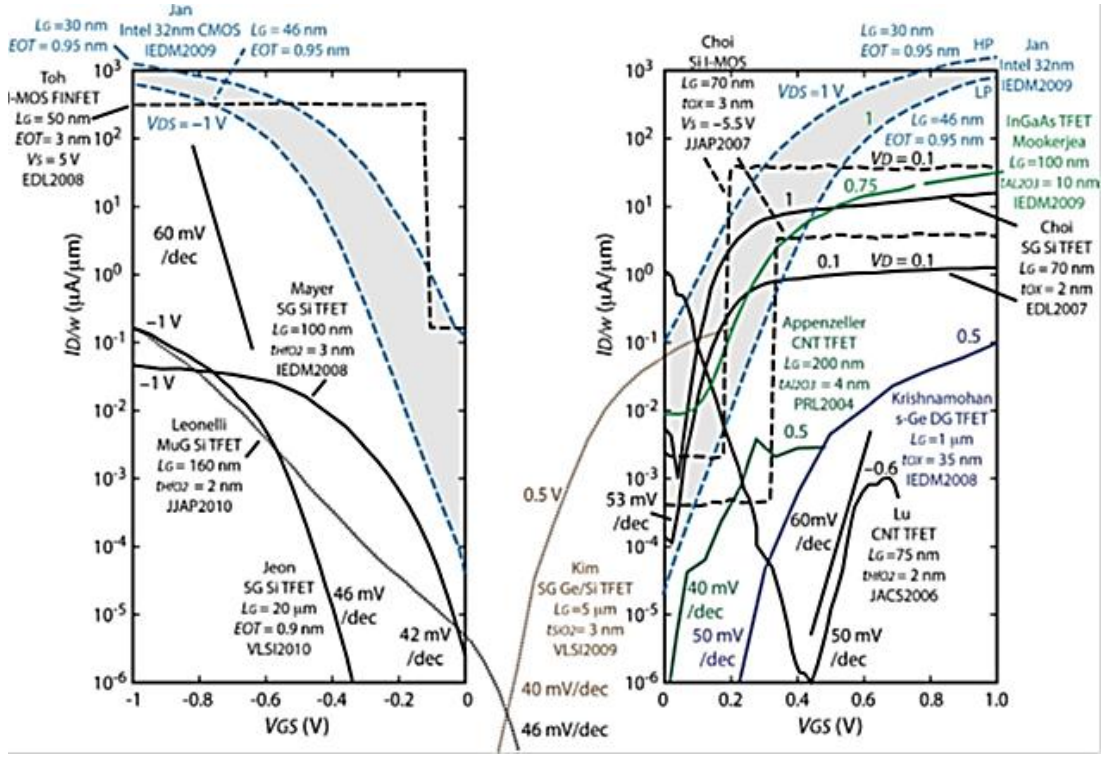

Figure 3 Comparison of published TFET channel current per unit width versus gate-to-source voltage for (a) p-channel and (b) n-channel transistors. Included are devices that show a subthreshold swing less than 60mV/decade or NDR in the forward characteristics of the tunnel junction. Dashed lines bordering the shaded area indicate measured high-performance (HP) and low-power (LP) 32-nm node MOSFET technology. The black dashed lines are measured characteristics for I-MOS transistors. For I-MOS, to plot on the same scale, the source voltage is shifted and the VGS indicated should be added to the listed source voltage to get the true gate-to-source voltage [2].

In most of the literature published so far, the experimentally shown ON-currents are unacceptably low for a technology that would like to replace the conventional MOSFET (hereafter, simply referred to as the MOSFET). While OFF-currents are in the range of femtoamperes or picoamperes, ON-currents for applied drain and gate voltages of 2 V are still limited to the nanoamperes range. Furthermore, in order to have a CMOS-compatible technology, voltages should be limited even more, to about 1.2 V. While one publication shows ON-currents up to 0.5mA/µm, these devices seem to be hybrid devices rather than pure Tunnel FETs, since their subthreshold slope is constant rather than Vg-dependent [9]. The Fig. 3, compiles measured n- and p-channel TFET drain current per micron gate width ID=w versus gate-to-source bias VGS, for a given drain-to-source bias VDS, against 32-nm node CMOS. For CMOS, both high-performance (HP) and low-power (LP) technologies are shown (dashed lines); these are measured values. For the purposes of this comparison, only TFETs that exhibit less than 60 mV/decade or NDR in the tunnel junction in the forward current direction are included. While the TFET on-current is not dependent on gate length, the gate length is indicated in the figure as well as gate oxide thickness or equivalent oxide thickness (EOT), to provide a scale for the experimental report. The subthreshold swings demonstrated thus far are not now in a current range of interest for either HP or LP applications as the low swings typically occur at less than 1 nA/um.

3. TFET Analysis

In comparison to traditional MOSFETs, the most exciting highlight is that TFETs exhibit lower sub-threshold swing and lower off current. A sub-threshold swing of 52.8mV/dec and off current of 10−14A/µm has been experimentally demonstrated in and even lower values have been predicted in simulation studies [1]. However, because of the use of the tunneling effect, the tunnel FET has the disadvantage that the current passing through it is smaller than that through the MOSFET. The challenge in TFET is to achieve high performance i.e. high I_{ON} without degrading I_{OFF}, combined with an S of less than 60 mV per decade. Also the unique characteristic of TFETs, referred to as unidirectional conduction, poses a significant challenge in the design of PTL (Pass transistor logic) and SRAM cell.

One of the major application constraints of the TFET is the unidirectional current-conduction characteristic. For logic circuits, the uni-directional characteristics does not present a serious problem, except for pas s transistor based circuits for which an TFET with opposite current conducting direction can be added at the expense of area/performance if bi-directional characteristics is required. For SRAMs, however, the uni-directional characteristics severely impact the robustness due to conflicting Read/Write requirements and stringent cell area constraint.

The fundamental requirement for PTL is that every device in the PTL stack should be able to source and sink

current when needed. TFETs are predominantly unidirectional devices that exhibit asymmetric current conduction. This inherent property of tunneling devices cannot be eliminated by structural or material changes.

For pass-transistor-based logic circuits, a TFET with an opposite current-conducting direction can be added at the expense of area/performance if bidirectional characteristic is required.

TFETs are only suitable to conduct current in one direction. This unique characteristic of TFETs, referred to as unidirectional conduction, poses a significant challenge in the design of the access transistors of the TFET SRAM since the access transistors are required to conduct current in both directions. For SRAM cells, however, the unidirectional characteristics severely impact robustness due to conflicting read/write requirements and the stringent cell-area constraint. TFET SRAM cells with a single-type access transistor for write suffered from the lack of push–pull action due to TFET's unidirectional conduction characteristics and large crossover contention from the holding transistor, resulting in insufficient WSNM and necessitating write-assist.

4. Conclusions

Today TFETs represent the most promising steep-slope switch candidate, having the potential to use a supply voltage significantly below 0.5V and thereby offering significant power dissipation savings. Because of their low off currents, they are ideally suited for low-power and low-standby-power logic applications operating at moderate frequencies (several hundred MHz). Other promising applications of TFETs include ultralow-power specialized analog integrated circuits with improved temperature stability and low-power SRAM.

The challenge in TFET is to achieve high performance i.e. high I_{ON} without degrading I_{OFF}, combined with an S of less than 60 mV per decade. Also the unique characteristic of TFETs, referred to as unidirectional conduction, poses a significant challenge in the design of PTL (Pass transistor logic) and SRAM.

References

Ravindhiran Mukundrajan, Matthew Cotter, Vinay Saripalli, Mary Jane Irwin, Suman Dattay and Vijaykrishnan Narayanan,Ultra Low Power Circuit Design using Tunnel FETs

Alan C. Seabaugh, and Qin Zhang (2010), Low-Voltage Tunnel Transistors for Beyond CMOS Logic, *IEEE* Vol. 98, No. 12

Yin-Nien Chen, Ming-Long Fan, Pi-Ho Hu, Ming-Fu Tsai, Chia-Hao Pao, Pin Su and Ching-Te Chuang(2012),A Comparative Analysis of Tunneling FET Circuit Switching Characteristics and SRAM Stability and Performance, *IEEE*

Yin-Nien Chen, Ming-Long Fan, Vita Pi-Ho Hu, Pin Su, and Ching-Te Chuang*(2013)*, Design and Analysis of Robust Tunneling FET SRAM *IEEE transactions on electron devices*, vol. 60, no. 3

Bhargav K. Mamilla, Rahul Mishra(2011), A III-V Group Tunnel FETs with Good Switching Characteristics and their Circuit Performance, IJECCT, Volume 1 Issue 2

Brindsa.A,K.Chakrapani(2012),Characterization of tunnel fet for ultra low power analog applications, *Journal of Theoretical and Applied Information Technology*,Vol. 42 No.2

www.gktoday.in

Adrian M. Ionescu & Heike Riel(2011),Tunnel field-effect transistors as energy-efficient electronic switches, *nature* Vol 479

Kathy Boucart and Adrian Mihai Ionescu,(2007), Double-Gate Tunnel FET With High-k Gate Dielectric,*IEEE Transactions on Electron Devices*, Vol54, NO 7.