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Research Article

SPWM Controlled Induction Motor Drive with Different Multilevel Converter Topologies: THD Analysis

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Abstract

This paper presents a scheme of induction motor drive application with various combinations of Multilevel inverters and with SPWM controlling technique. In each combination along with motor performance characteristics analysis of the THD content of the multi level converter had given high priority. The converter topology power circuits contains PV cell and stand alone battery which explains the need of renewable energy sources utilization in drives scenario. As the number of levels increase in the output voltage, the THD content decreases and hence power quality increases. However there is a limit beyond which increasing the number of level is not economical and adoptable. Comparison of each topology with respect to THD content been tabulated. Matlab/Simulink is used to simulate the system.

Keywords: *Induction motor, Multilevel inverter, Energy management, PVcell, Multilevel SPWM, THD.*

1. Introduction

Among various electric motors Induction motor is very robustive, constant speed and satisfactory efficiency machine. It is the mostly adopted machine by the industry. The controlling of speed of the induction motor is also simple. In economical view also it is preferable to adopt the Induction motor drive. In different controlling techniques sinusoidal pulse width modulation is simple and easy way to control multi level inverters. SPWM generates least harmonics compared to remaining techniques. Nowadays power requirement of industry is increasing very much faster. The rapid evolution in the semiconductor devices and designers orientation leads to new topologies of Multilevel inverters. The Multilevel inverters are preferred for high power applications. Their control is much more complex and these techniques are still not widely used in the industry. The Multi level converter topology contains less THD content and in this paper two topologies i.e. Neutral point clamped multilevel inverter & cascaded H-Bridge multi level inverter been considered. In the above mentioned two techniques NPC is the old and fundamental topology but it is complicated in the analysis concern.

2. Photovoltaic system

The PVcell with versatile standalone battery is used to feed the induction motor in one topology. In remote areas to supply power for the loads PVcell is only the option. PVcell is been simulated by using its equivalent circuit. A stand alone battery bank is used to compensate the energy requirements needed by the induction motor. When PVcell is more than required additional energy is used to charge the battery. If it is below the limit additional energy will be taken from battery bank. This ups and downs of PVcell is due to solar radiation variance.

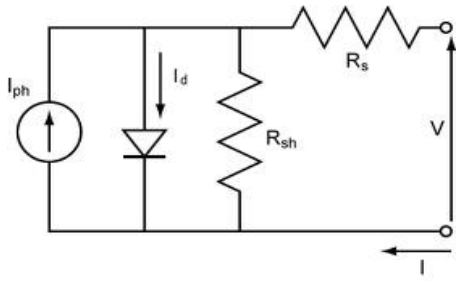

Fig.1: Equivalent circuit of solar PV

As shown in the fig-1, I_{Ph} is the short circuit current of PV cell and R_S is the series resistance, R_{Sh} is the shunt resistance, I_d is the diode current. The operation of PV cell is characterized by the fallowing equation

$$I=I_{Ph}-I_0[e^{\frac{qV+IR_S}{AKT}}-1]-\frac{V+IR_S}{R_{Sh}} \quad (1)$$

Where,
$\mathbf{I_{Ph}}$= Photo-generated current (A)

I= Cell output current (A)
I_0=Diode Saturation Current (A)
V=Cell Output Voltage (V)
Rs=Series Resistor (Ω)
e= Electron Charge 1.6×10-19 (coul)

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K=Boltzmann Constant (j/K)
T=cell temperature

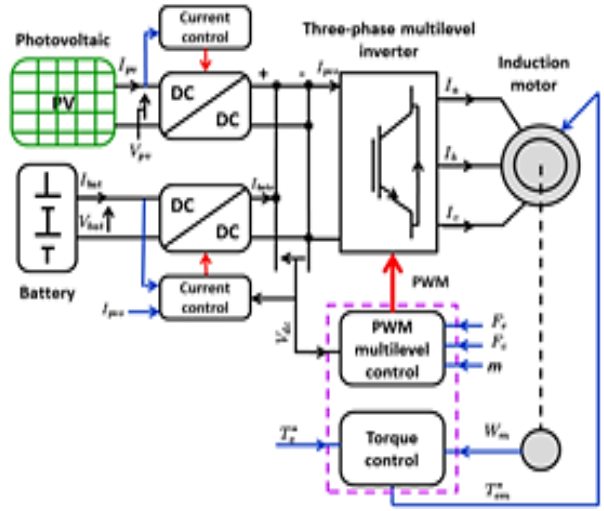


Fig. 2: Induction motor driven by PV-batteries standalone system using a controlled multilevel inverter.

3. Multilevel Inverter Control Strategies

A. The three-level inverter control strategy:

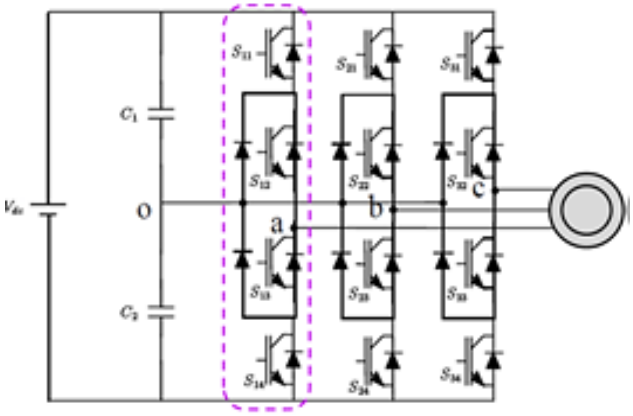


Fig. 3: Three-level three phase inverter

Fig (3) shows a three phase three level inverter.V_{ao} is the phase voltage between phase a and neutral 'o'.The three level NPC inverter is used for medium voltage, high power application. These '3' sequences are applied periodically .In SPWM technique the modulating wave is compared with reference waves both in the +ve and –ve halves. The comparator output is sent to the switches to generate phase output voltages.

Sequence	Switches State		Output phase(v_{ao})
	ON	OFF	voltage
1	S_{11},S_{12}	S_{13}, S_{14}	$+v_{dc}/2$
2	S_{12},S_{13}	S_{11}, S_{14}	0
3	S_{13}, S_{14}	S_{11},S_{12}	$-v_{dc}/2$

4. Cascaded H-Bridge Inverter

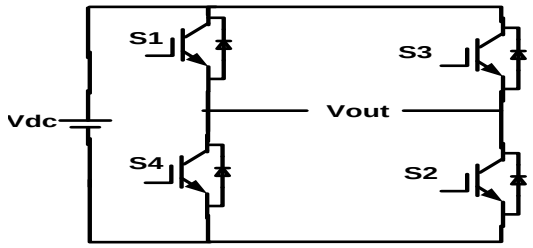


Fig. 4 Circuit of the single cascaded H-Bridge Inverter

For the above single phase three level inverter the switch positions and the output voltages are as follows.

Switches		Voltage Level
ON state	OFF state	
S1,S2	S3,S4	+Vdc
S3,S4	S1,S2	-Vdc
S4,D2	S3,D1	0

In the cascaded H-bridge inverter
Output voltage level=2x+1
Voltage step of each level=Vdc/(2x)
Where x=no of cascaded H-bridges
No. of H bridges are cascaded to get the the required level in the output voltage waveform.
The available PWM techniques for CHB inverter are
(1). Phase Shifted PWM (PSCPWM)
(2). Level shifted PWM (LSCPWM)

Phase Shifted PWM (PSCPWM)

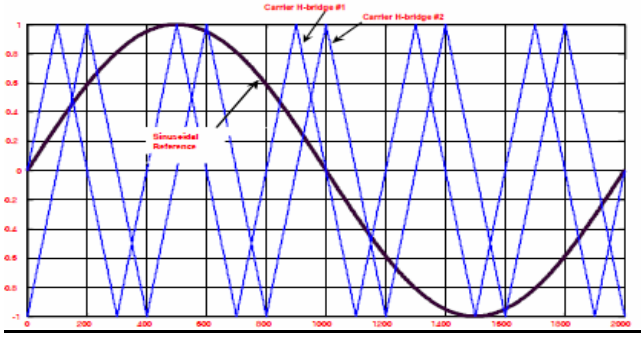


Fig.5: Phase Shifted Carrier PW

For Y voltage levels (Y-1) carrier signal required and they are phase shifted with an angle θ=(360°/Y-1).The gate signals are generated with proper comparison of carrier wave and modulating signal.

Level shifted PWM (LSCPWM)

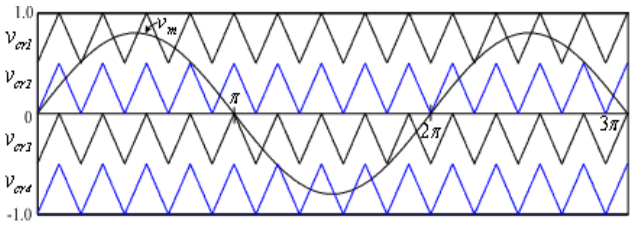


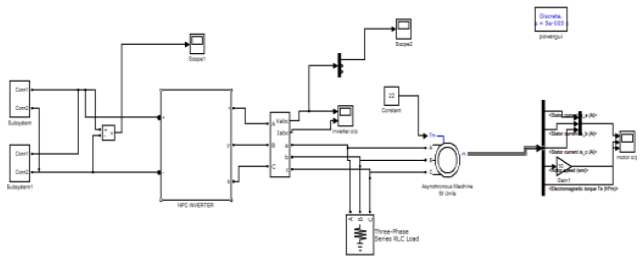
Fig.6: Level Shifted Carrier PW

For carriers signals, the time values of each carrier waves are set to [0 1/600 1/300] while the outputs values are set according to the disposition of carrier waves. After comparing, the output signals of comparator are transmitted to the IGBT.

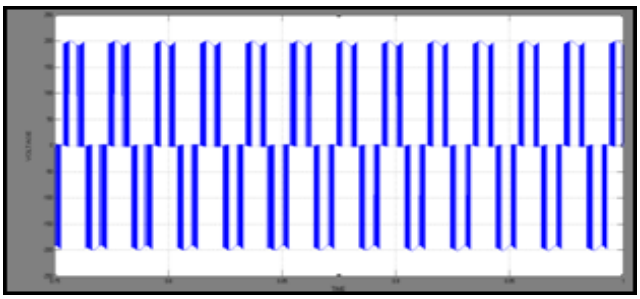
5. Matlab Modeling and Simulation Results

Here simulation is carried out in two different configurations, (1). Implementation of Proposed Concept using Neutral Clamped Type Multilevel Inverter. (2) Implementation of Proposed Concept using Cascaded H-Bridge Multilevel Type Inverter.

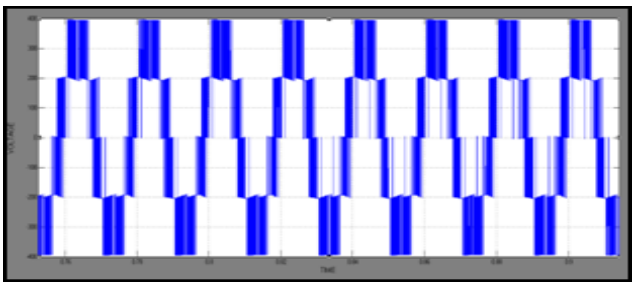
Case I: Implementation of proposed concept using neutral clamped type multilevel Inverter.



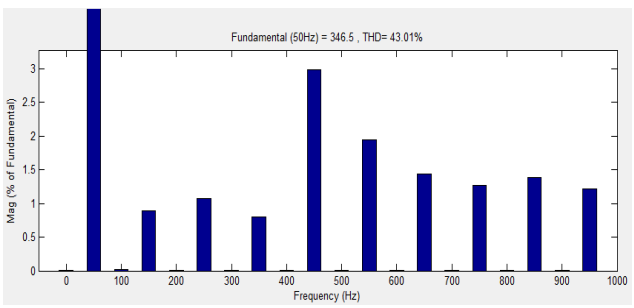
Phase voltage



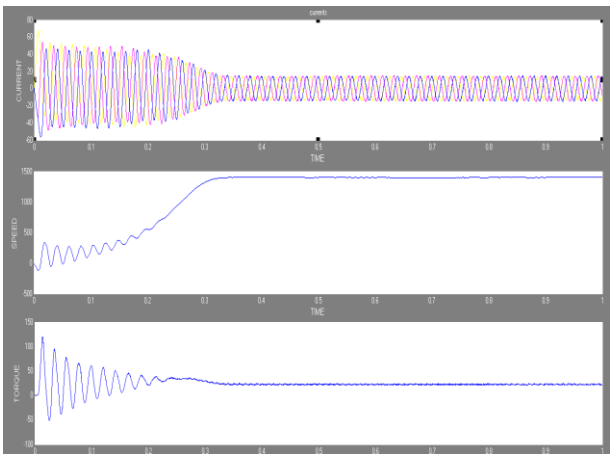
Line voltage:



THD (Phase voltage):

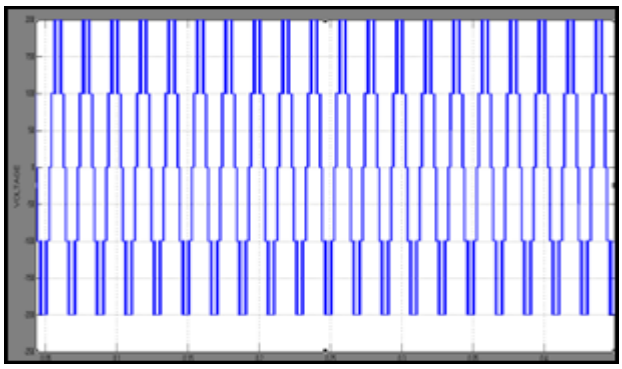


Motor Performance Characteristics

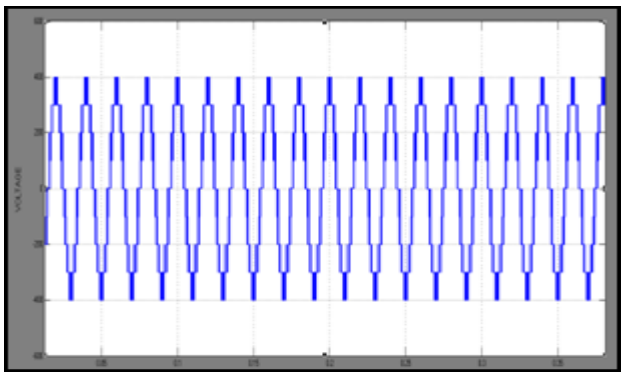


5 Levels

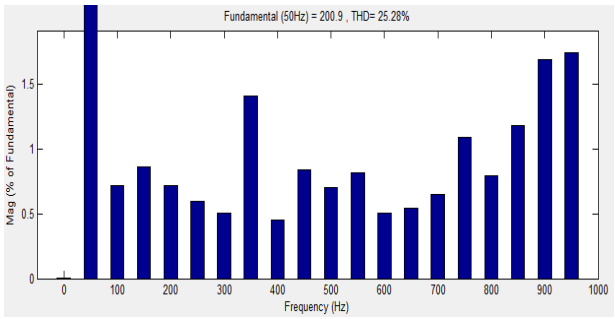
Phase voltage:



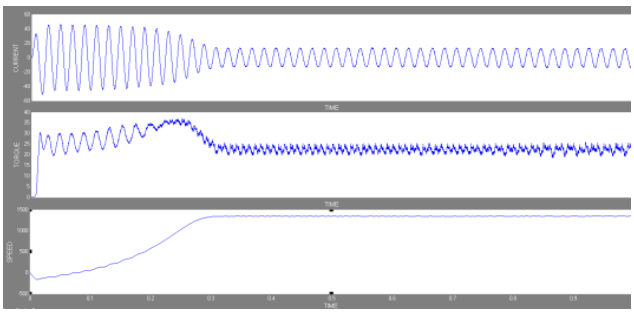
Line voltage:



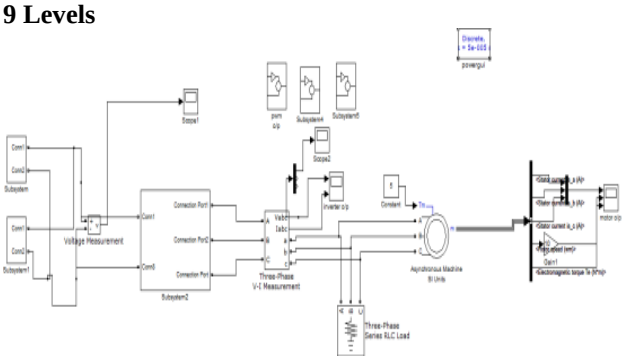
THD (Phase voltage):



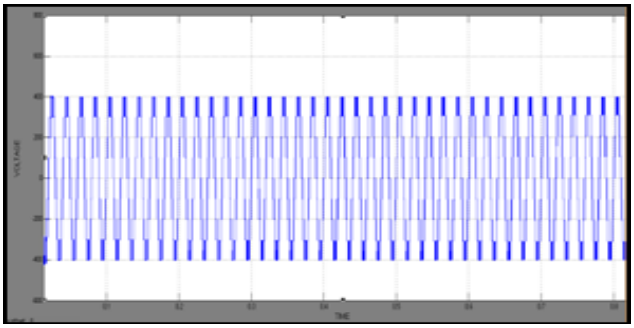
Motor Performance Characteristics



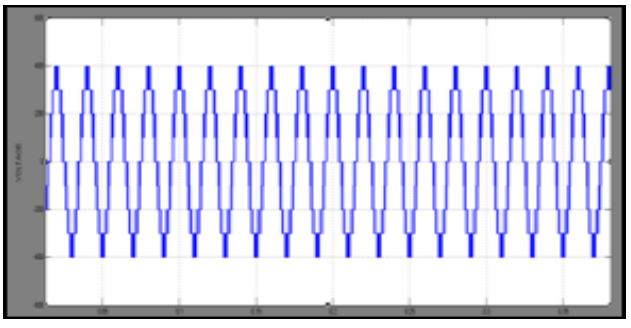
9 Levels



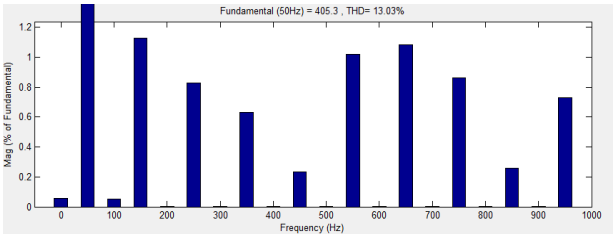
Phase voltage:



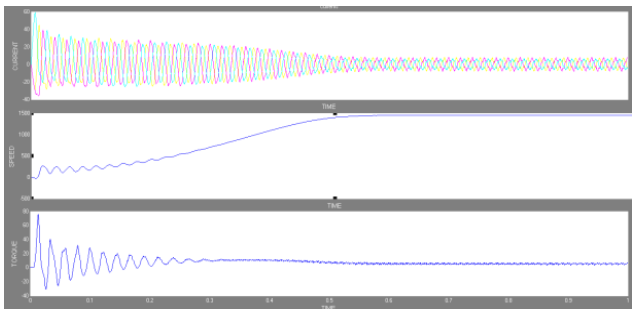
Line voltage:



THD (Phase voltage)



Motor Performance Characteristics



Comparison of two Topologies THD

Neutral Point Clamped		Cascaded H-Bridge	
Level	THD	Level	THD
3	43.01%	3	44.49%
5	25.28%	5	25.28%
9	13.03%	9	13.21%

Conclusion

In this paper 3,5,9 level induction motor drive is been developed and simulated. The THD content for full load condition of motor has been tabulated. The main two topologies analyzed in this paper are NPC and CHB. Observing simulation results it is concluded that two topologies gives almost same THD but in designing CHB is simple so it is preferable compared to NPC. The maximum level of output voltage for medium power range drives are 9 further increasing the no of level is not economical and adoptable. As the level increases THD content of stator currents decreases which in turn reduces the heat content of stator coils and also increases the effective life of Induction motor.

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