

Research Article

## Implementation of Energy-Efficient Input Buffer for NoC Router

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### Abstract

Network-on-Chip (NoC) is an efficient solution for interconnection between processor cores in Chip Multi-Processor (CMP), which will consume extra energy. This paper is focusing on the energy-efficient design of input buffers, one of the most critical components in NoC. The energy efficient input buffer is proposed for NoC routers which reduce energy consumption more significantly as compared to conventional input buffer and also give reduction in delay. We use a 65nm CMOS process in our simulation.

**Keywords:** Buffer, NoC, SoC

### Introduction

Network-on-Chip (NoC) is an appealing alternative for communication in SoCs with ability of providing high throughput, low latency and scalability. Using a network to replace global wiring has advantages of structure, performance, and modularity (Son Truong Nguyen *et al*).

NOC architectures are based on packet-switched networks. This has led to new and efficient principles for design of routers for NOC. For circuit-switched networks, routers may be designed with no queuing (buffering). For packet-switched networks, some amount of buffering is needed, to support bursty data transfers. Buffers can be provided at the input, at the output, or at both input and output (E. Rijpkema *et al*,2003). NoC architecture has two parts: router and data link. The router is a module which can use to store and forward data, and the data link use to transmit signals from one router to its neighbour. and as given in the figure there are three parts in one router module: input buffer, arbiter, and crossbar. The input buffer stores the input data temporarily, and obviously each direction should hold one input buffer queue (up, down, left, right, and home, totally five directions) because router is connected to another router in five direction south, east, west, north and local i.e. Home. The architecture of NoC cannot be very complex, so the topology and the routing algorithm of NoC is often simple, for example, 2D mesh or 2D torus, thus the routing algorithm is correspondingly XY or TXY algorithm. The two algorithms are both simple and can be decided in early stage of the router pipeline. So the delay of arbiter is not critical and its energy consumption is very small compared to input buffer, crossbar and data link, so it is ignored in

our evaluation (Amit Kumary *et al*). It is observed that the probability the signals transmitted on NoC are zero is bigger than the probability the signals are one (Jun Wang *et al*). This paper proposes an energy-efficient input buffer of NoC, which make use of the mentioned NoC characteristics. The energy of the NoC will be reduced using this energy efficient circuit with simulation in 65 nm cmos process.

### Literature Review

#### NOC router Architecture

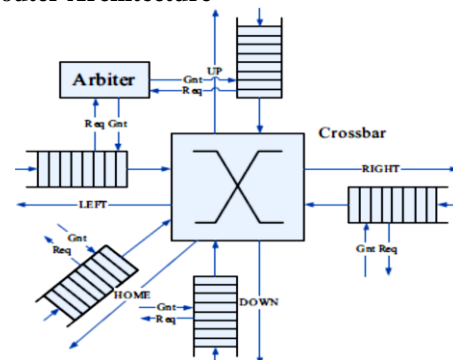


Figure 1 Architecture of NoC

As we can see that there are three parts in one router Architecture are as: input buffer, arbiter, and crossbar. The input buffer stores the input data temporarily, and obviously each direction should hold one input buffer queue (up, down, left, right, and home, totally five directions). Usually the destination node of the request is easy to be decided, so the next hop can be decided when the input data enters input buffer. The arbiter receives requests from input buffers and allocates virtual channels

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to requests and then gives grant signals to request initiators. The crossbar switches granted input requests and forwards the request data to data link, and then the request data is transmitted to the next hop router through data link. Crosspoint matrix is the important and central component of router. It consists of various multiplexers and demultiplexers and interconnection of all 5 input channels and 5 output channel. It allows all five connections at the same time by configuring input and output channel. The control of crosspoint matrix is under output channel as while granting the request of any input channel, output channel configures the multiplexers and demultiplexers of it.

### Buffer Architecture

It consists of the following major blocks.

**Flit payload buffer:** This unit consists of buffers at each input port which are addressed in units of its (128 bits each) and store all its arriving at an input port before they are switched out of the router.

**Header control block (HCB)** In our dynamically managed buffer design, since flits of a particular packet be assigned non-contiguously within the payload buffer, the header control block contains an entry for each packet which serves to track the flits within that packet by storing the pointers where the respective flits are stored. In addition, the header control block also stores routing information related to a packet including its message (or traffic) class and output port.

**Buffer management unit:** This unit consists of the buffer allocator and the flow control manager. The buffer allocator is responsible for assigning a free buffer to each incoming flit. This is done by maintaining a list of free buffer entries and assigning the buffer at the top of this list to any incoming flit. The flow control manager is responsible for signaling buffer availability to the upstream router. We use on/off flow control for this purpose. A free buffer count is maintained to count the total number of free buffers.

**Packet forwarding unit:** This helps implement the FLO feature of our switch allocator (where successive request from flits of the same packet are prioritized) by retrieving successive buffer pointers from the same entry of the header control block corresponding to flits within the same packet.

### Need of Energy Efficient input Buffer

The architecture of NoC cannot be very complex. So the delay of input buffer and its energy consumption is very high. The proposed architecture make use of the characteristics of NoC which the probability the signals transmitted on NoC are 0 is bigger than the probability the signals are 1. The power consumption of input buffer reading and writing 0 is less than the power consumption of input buffer reading and writing 1. This energy efficient circuit can reduce energy consumption of NoC by about 50%.

### Characteristics of Transmission Data on NoC

The digital signals transmitted on NoC are occurred by cache coherence protocol. The directory-based coherence protocol usually occurs eleven types of requests and responses: read shared, read exclusive, upgrade, write back eliminate, intervention shared, intervention exclusive, invalidate, ACK, ACK with data, NACK. The digital signals of these requests and responses can be regarded as three kinds: data, physical address, and control information like initiator ID and MSHR ID. Some requests and responses only contain physical address and control information, and some contain all three kinds of information. We can only think of the data information because the data is of the biggest bit width and is much more than address information and control information. By analyzing these kinds of information, we can find the characteristics of these digital signals transmitted on NoC that the probability the signals transmitted on NoC are zero is bigger than the probability the signals are one. There are some reasons for explaining this phenomenon: For all, the data information transmitted on NoC includes newest copy of level one instruction and data cache of processing core. For instruction cache copy, there are some entries of instruction format is probably zero because immediate values, address offsets and branch displacements are often small integers. For data cache copy, zero and small integers are often used to represent flags, array indexes, and synchronization variables, and some dynamic allocated variables are set to zero when initialization.

### Energy efficient circuit design

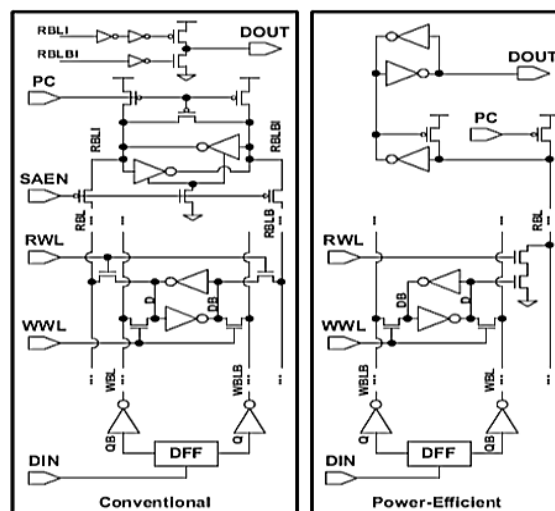


Figure 2 Circuit of conventional and power efficient input buffer

Since the energy consumption of an operation depends on the data of current cycle as well as its continuously previous cycle, we use the data transition as the independent variable for precision. For example, we use four different kinds of data Transitions, 0→0, 0→1, 1→1,

1→0, to describe the energy consumption of an read operation for input buffer, which mean read 0 after 0, read 1 after 0, read 1 after 1, read 0 after 1, respectively. So the energy consumption of transmitting 1-bit data from one node to the next will be discussed as: write data into the input buffer.  $E_{write}$ ; read data from the input buffer  $E_{read}$ .

### Write

The write circuit of zero-efficient design is exactly the same as conventional. Differential write bitlines (WBL) are driven by static logic inverters. So the energy consumption of writing 1-bit data is

$$E_{write\_cv} = E_{write\_ze} = f(e_{w0}, e_{w1}, e_{wl})$$

$$\text{Where } e_{w0} = (E_{wdec} + E_{wwl}) / W_{bit}; e_{w1} = E_{wbl} + E_{cc}$$

And  $W_{bit}$  is data width of the input buffer in bit;  $E_{wdec}$  is the energy consumed by write address input flipflops and decoder;  $E_{wwl}$  is consumed while charging write word-line (WWL);  $E_{wbl}$  is consumed by charging or discharging differential write-bit-lines (WBL);  $E_{cc}$  is consumed while the input data is different from the data stored in the bit cell. Because of the characteristic of input buffer, the enabled input write address in one cycle will not be the same as its previous, so  $E_{wdec}$  and  $E_{wwl}$  will be counted in for each write operation. And  $E_{cc}$  is ignored because it is very small compared to the others.

### Read

As in the conventional design, differential RBL's will be pre-charged by the PC signal at the rising edges of clock while the read function is enabled, and one of them will be discharged according to the stored data (D & DB) when read word-line (RWL) rises. After that, in the evaluation period, the voltage difference between RBL's is evaluated and output data is generated. And due to differential RBL's, no matter what the data transition is, the energy consumption of reading 1-bit data is the same. So the energy consumption of reading 1-bit data from conventional input buffer is

$$E_{read\_cv} = (E_{rdec} + E_{rwl\_cv} + E_{rpcg\_cv}) / W_{bit} + E_{rpc\_cv} + E_{rev}$$

Where  $E_{rdec}$  is the energy consumed by read address input flip-flops and decoder;  $E_{rwl}$  is consumed by charging RWL;  $E_{rpcg\_cv}$  is consumed while generating pre-charge signal;  $E_{pc\_cv}$  is consumed while pre-charging RBL's;  $E_{rev}$  is consumed during evaluation and generation of output data by the sense amplifier; The same reason as write operation,  $E_{rdec}$  and  $E_{rwl}$  will be counted in for each read operation also. In Energy-efficient design, the differential read bit-lines (RBL) are reduced to single-bit. The pre-charged single-bit RBL will be discharged only if the stored data (D) is 1. So the

energy consumption of reading 1-bit data from power-efficient input buffer is

$$E_{read\_ze} = h(e_{r3}, E_{rdc}, E_{rpc})$$

$$\text{Where } e_{r3} = (E_{rdec} + E_{rwl\_ze} + E_{rpcg\_ze}) / W_{bit}$$

$E_{rwl\_ze}$ ,  $E_{rpcg\_ze}$  and  $E_{rpc\_ze}$  have the same meaning as  $E_{rwl\_cv}$ ,  $E_{rpcg\_cv}$  and  $E_{rpc\_cv}$ , respectively, but are different in value. And  $E_{dc}$  is consumed while discharging the RBL and generating output data.

### Problem Definition

In NoC Router energy consumption is major issue while designing. In Noc Router one third of energy is consumed by buffer. In Conventional circuit of input buffer, energy is more consumed, So we will be implemented energy efficient input buffer circuit. In NoC the digital signals of requests and responses can be regarded as three kinds: data, physical address, and control information. Some requests and responses only contain physical address and control information, and some contain all three kinds of information. We can only think of the data information because the data is of the biggest bit width and is much more than address information and control information. By analyzing these kinds of information, we can find that characteristics of digital signals transmitted on NoC that the probability of signals transmitted on NoC are zero is bigger than the probability the signals are one. The energy consumption of input buffer reading and writing 0 is less than the energy consumption of input buffer reading and writing 1. We will use simulate the design of conventional and energy efficient input buffer circuit in 65 nm technology. We will compare parameter energy along with delay and also counting of gates.

### Proposed Work

- We will use Tanner software to design conventional and energy efficient input buffer circuit.
- In this we will design the circuit by using different technology i.e 180 nm and 90 nm and 65 nm.
- We will be compare parameter energy along with delay and chip area with the help of these two technology.

### Proposed Methodology

We will use the methodology of probability of transmitting the signal zero on NoC is bigger than probability of signal are one because energy consumption of input buffer reading and writing 0 is less than energy consumption of reading and writing 1.

### Implication

As we will design energy efficient input buffer in NoC

router. This can improve energy efficiency of NoC router more significantly as we use 65 nm cmos process.

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