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Research Article

Dual Port SRAM

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Abstract

Large SRAM arrays that are widely used as cache memory in microprocessors and application-specific integrated circuits can occupy a significant portion of the die area..In an attempt to optimize the performance of such chips, large arrays of fast SRAM help to boost the system performance. The demand for static random- access memory (SRAM) is increasing with large use of SRAM in mobile products, System On-Chip (SoC) and high-performance VLSI circuits.70% of the System On-Chip (SoC) uses SRAM memory. SRAM is significant component used for the cache memory in microprocessors, main frame computers, engineering workstations and memory in hand-held devices due to high speed and low power consumption. The main objective of this project is to design and implement Dual Port SRAM Memory using 180nm CMOS technology. The work includes designing of write and read circuit. The Dual Port SRAM is capable of storing 2 bits with operating voltage of 1.8v.To design and implement SRAM Memory array Standard GPDK180(General Purpose Design Kit) technology library is used. The proposed work is designed using Cadence Tool.

Keywords: *Dual port SRM etc.*

1. Introduction

a. Memory

Modern digital systems require the capability of storing and retrieving large amounts of information at high speeds. Memories are circuits or systems that store digital information in large quantity. This chapter addresses the analysis and design of VLSI memories, commonly known as semiconductor memories. Today, memory circuits come in different forms including SRAM, DRAM, ROM, EPROM, EPROM and Flash. While each form has a different cell design, the basic structure, organization, and access mechanisms are largely the same. In this chapter, one can classify the types of memory, and focus on the static RAM design .

b. Types of Memory

Read-write random-access memories (RAM) may store information in flip-flop style circuits or simply as charge on capacitors. Approximately equal delays are encountered in reading or writing data. Because read-write memories store data in active circuits, they are volatile; that is, stored information is lost if the power supply is interrupted. The natural abbreviation for read-write memory would be RWM. However, pronunciation of this acronym is difficult. Instead, the term RAM is commonly used to refer to read-write random-access memories. If the terms were consistent, both read-only and read-write memories would be called RAMs. The two most common types of RAMs are the static RAM (SRAM) and the dynamic RAM (DRAM). Static RAMs hold the stored value in flip- flop circuits as long as the power is on. SRAMs tend to be high-speed memories with clock cycles in the range of 5 to 50 ns. Dynamic RAMs store values on capacitors. They are prone to noise and leakage problems, and are slower than SRAMs, clocking at 50 ns to 200 ns. However, DRAMs are much denser than SRAMs up to four times denser in a given generation of technology. Read-only memories (ROMs) store information according to the presence or absence of transistors joining rows to columns. ROMs also employ the organization and have read speeds comparable to those for read-write memories. All ROMs are nonvolatile, but they vary in the method used to enter (write) stored data. The simplest form of ROM is programmed when it is manufactured by formation of physical patterns on the chip; subsequent changes of stored data are impossible. These are termed mask-programmed ROMs. In contrast, programmable read-only memories (PROMs) have a data path present between every row and column when manufactured, corresponding to a stored 1 in every data position. Storage cells are selectively switched to the 0 state once after manufacture by applying appropriate electrical pulses to selectively open (blow out) row-column data paths. Once programmed, or blown, a 0 cannot be changed back to logic1.

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Erasable programmable read-only memories (EPROMs) also have all bits initially in one binary state. They are programmed electrically (similar to the PROM), but all bits may be erased (returned to the initial state) by exposure to ultraviolet (UV) light. The packages for these components have transparent windows over the chip to permit the UV irradiation. Electrically erasable programmable read-only memories (EEPROMs, EPROM, or E-squared PROMs) may be written and erased by electrical means. These are the most advanced and most expensive form of PROM. Unlike EPROMs, this must be totally erased and rewritten to change even a single bit, EPROMs may be selectively erased. Writing and erasing operations for all PROMs require times ranging from microseconds to milliseconds. However, all PROMs retain stored data when power is turned off; thus they are termed nonvolatile. A recent form of memory is termed as Flash memory, a name derived from the fact that blocks of memory may be erased simultaneously. Flash memory is written using the hot-electron effect whereas EPROM is written using Fowler-Nordheim (FN) tunneling. Both types are erased using FN tunneling. Their large storage capacity has made this an emerging mass storage medium. In addition, these types of memories are beginning to replace the role of ROMs on many chips, although additional processing is required to manufacture Flash memories in a standard CMOS technology.

Table 1.1: Comparison of Memories.

	DRAM	SRAM	UV EPROM	EEPROM	Flash
Data Volatility	Yes	Yes	No	No	No
Data Refresh Operation	Required	No	No	No	No
Cell Structure	IT-IC	6T	IT	2T	1T
Cell Density	High	Low	High	Low	High
Power Consumption	High	High/Low	Low	Low	Low
Read Speed (latency)	50ns	10/70ns	50ns	50ns	50ns
Write Speed	40ns	5/40ns	10s	5ms	(10s-1ms)
Endurance	High	High	High	Low	High
Cost	Low	High	Low	High	Low
In-System writ ability	Yes	Yes	No	Yes	Yes
Power Supply	Single	Single	Single	Multiple	Single
Application example	Main Memory	Cache/ PDA	game Machines	ID Card	Memory card

As microprocessors and other electronics applications get faster and faster, the need for large quantities of data at very high speeds increases, while providing the data at such high speeds gets more difficult to accomplish. As microprocessor speeds increase from 25 MHz to 100 MHz, to250 MHz and beyond, systems designers have become more creative in their use of cache memory, interleaving, burst mode and other high-speed methods for accessing memory. The old systems sporting just an on-chip instruction cache, a moderate amount of DRAM and a hard drive have given way to sophisticated designs using multilevel memory architectures. One of the primary building blocks of the multi-level memory architecture is the data. In SOC (System on chip) the processor has on chip memory which increases the speed of the processor drastically and it is implemented using SRAM.

c. Features Of SRAM:

1) Data is stored as long as supply is applied
2) Fast - so used where speed is important (e.g., caches)
3) Differential outputs
4) Low power consumption
5) Compatible with CMOS technology

d. Why SRAM?

SRAM cells are usually used to implement memories that require short access times, low power dissipation, and tolerance to environmental conditions. There are many reasons to use an SRAM or a DRAM in a system design. Design tradeoffs include density, speed, volatility, cost, and features. All of these factors should be considered before you select a RAM for your system design [1].

1) Speed - The primary advantage of an SRAM over a DRAM is its speed. The fastest DRAMs on the market still require five to ten processor clock cycles to access the first bit of data. Fast, synchronous SRAMs can operate at processor speeds of 250 MHz and beyond, with access and cycle times equal to the clock cycle used by the microprocessor. With a well designed cache using ultra-fast SRAMs, conditions in which the processor has to wait for a DRAM access become rare.

2) Density - Because of the way DRAM and SRAM memory cells are designed, readily available DRAMs have significantly higher densities than the largest SRAMs. Thus, when 64 Mb DRAMs are rolling of the production lines, the largest SRAMs are expected to be only 16 Mb.

3) Volatility - While SRAM memory cells require more space on the silicon chip, they have other advantages that translate directly into improved performance. Unlike DRAMs, SRAM cells do not need to be refreshed. This means they are available for reading and writing data 100% of the time.

4) Cost - If cost is the primary factor in a memory design, then DRAMs win hands down. If, on the other hand, performance is a critical factor, then a well-designed SRAM is an effective cost performance solution.

5) Custom features - Most DRAMs come in only one or two flavors. This keeps the cost down, but doesn't help when you need a particular kind of addressing sequence, or some other custom feature. SRAMs are tailored, via metal and substrate, for the processor or application that will be using them. Features are connected or disconnected according to the requirements of the user. Likewise, interface levels are selected to match the processor levels

2. Study of Single Port Sram Cell

a. Memory Cell

Memory cells are the key components of any SRAM unit. An SRAM cell can store one bit of data. An SRAM cell comprises two back-to-back connected inverters forming a latch and two access transistors. Access transistors serve

for read and write access to the cell. An SRAM cell offers the following basic parameters.

1) Retention - An SRAM cell is able to retain the data indefinitely as long as it is powered.

2) Read - An SRAM cell is able to communicate its data. This operation does not affect the data i.e., Read operation is non-destructive.

3) Write - The data of an SRAM cell can be set to any binary value regardless of its original data.

A number of SRAM cell topologies have been reported in the past decade. Among these topologies, resistive load four-transistor (4T) cell, load less 4T cell and six transistor (6T) SRAM cell have received attention in practice, owing to their symmetry in storing logic `one' and logic `zero'. The data retention in the 4T SRAM cells is ensured by the leakage current of the access transistors. Hence, they are not proper candidates for low- power applications. On the other hand, the data stability in a 6T SRAM cell is independent of the leakage current. Moreover,

6Tcon_guration exhibits a significantly higher tolerance against noise which is an important benefit especially in the scaled technologies where the noise margins are shrinking. That is the main reason for the popularity of the 6T SRAM cell in low-power SRAM units instead of the 4T configurations.

b. Memory Cell Operation

A 6T SRAM cell consists of two cross- coupled CMOS inverters and two access transistors. The output (input) of the inverters construct the internal nodes of the cell. Once active, the access transistor facilitates the communication of the cell internal nodes with the input/output ports of the cell. The input/output ports of the cell are called bit lines (BL and BLbar) Bit lines are a shared data communications medium among the cells on the same column in an array of cells. Consequently, they have high capacitive loading. The read and write operations are conducted through the bit lines .

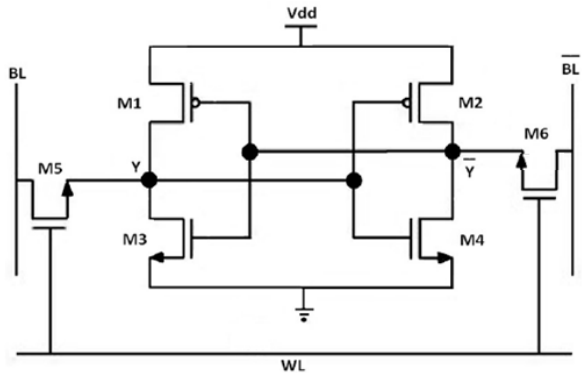

Fig 1.6 T Cell

Single bit SRAM memory cell is shown in Fig3.1 Static latches are used in the SRAM cell. SRAM cell is made up of flip flop comprising of two cross coupled inverters. Two access transistors are used to access the stored data in the cell. These transistors are turned ON/OFF by the control line called word line (WL). Generally this word line is connected to the output of row decoder circuits. When WL=Vdd the SRAM cell is connected to bit line (BL) and complement of bit line (BLbar) allowing both read and write operations. Read-write operation is carried out by the help of access transistors.

1) Read Operation: Consider node Y as reference node of the SRAM cell. Cell is said to be storing 1 if node Y is high at Vdd and node Y bar is at 0V. For the reverse voltage conditions cell is said to be storing zero. Let us assume that cell is storing 1.Before the read operation starts BL and BL bar lines are precharged to Vdd/2. When the WL is activated the current flows through M5 and M6. Now current from Vdd will flow through M1 and M5 charging the bit line capacitance, say CBL. The existing capacitance on the line BL, say CBLbar discharges through the transistors M6 and M4.This process develops a voltage difference between node Y and node Y bar which is sensed by the sense amplifier to detect it as 1. Similarly a 0 in the cell is also detected by the sense amplifier.

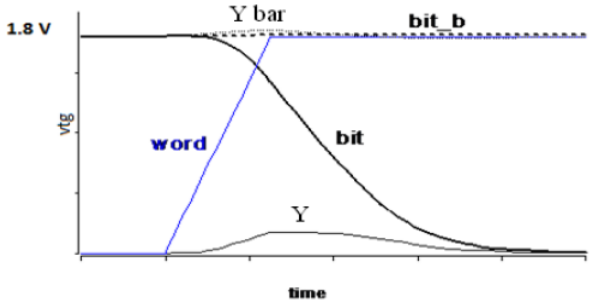

Fig. 2 Read operation

2) Write Operation

Let us consider the write operation of zero to the cell which is storing a value of 1. For this, sense amplifiers and precharged circuits are disabled. The cell is selected by activating the corresponding WL signal. To write zero to the cell, BL line held low and BL bar line is raised to Vdd by the write circuit. Thus the node Ybar is pulled up towards the Vdd/2 while node Y is pulled down to Vdd/2. When the voltage crosses this level on two nodes feedback action starts parasitic capacitances developed by M3, M5 and M4, M6 are charged and discharged respectively. Ultimately node Y stabilizes at the value 1. Since these parasitic capacitances offered by transistors are comparatively much lesser than the bit line capacitances, write operation is faster than read operation.

SRAMs can be organized as bit-oriented or word-oriented. In a bit-oriented SRAM, each address accesses a single bit, whereas in a word oriented memory, each address addresses a word of n bits (where the popular values of n include 8, 16, 32 or 64). Column decoders or column MUXs (YMUXs) addressed by Y address bits allow sharing of a single sense amplifier among 2,4or more columns. An SRAM cell

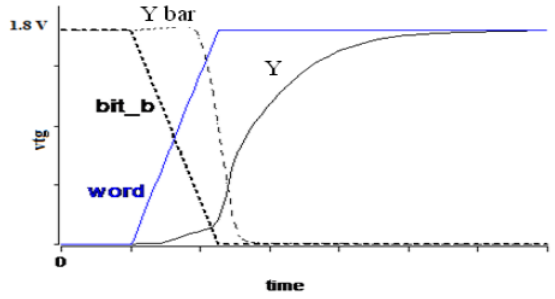

Fig. 3 Write operation

SRAM Block Structure

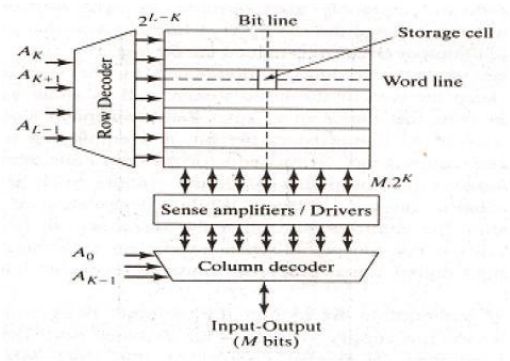

Fig. 4 General SRAM array structure

must be designed such that it provides a non-destructive read operation and a reliable write operation. These two requirements impose contradicting requirements on SRAM cell transistor sizing. SRAM cell transistor sizes are calculated using below equation.

$$\frac{(W/L)n}{(W/L)p} = \frac{2(VDD-1.5Vtn)Vtn}{(VDD-2Vtn)2}$$

3. **Design Of Dual Port SRAM Cell**

a. Dual Port Sram Cell

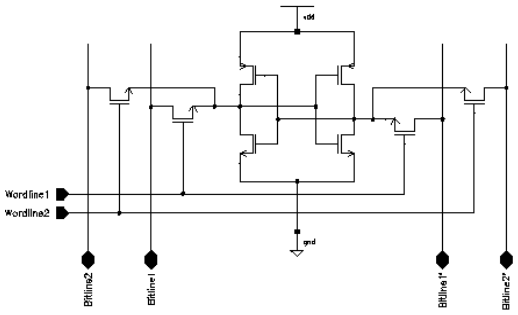

Fig. 5 Dual Port SRAM

Dual Port SRAM cell design considerations are important for a number of reasons. Firstly, the design of a Dual Port SRAM cell is key to ensure stable and robust SRAM operation. Secondly, owing to continuous drive to enhance the on-chip storage capacity, the SRAM designers are motivated to increase the packing density. Therefore, an SRAM cell must be as small as possible while meeting the stability, speed, power and yield constraints. Dual Port SRAM cell is the component to store binary information. It has both read and write capabilities. The word line defines operational modes.

1) When both Wordline1=Wordline2=0, both access transistors are off and cell is isolated. To perform read operation.
2) When Worldline1=1 and Worldline2=0, the Bitline1 is selected and perform the write operation.
3) When Worldline1=0 and Worldline2=1, the Bitline2 is selected and perform the write operation.
4) When Worldline1=1 and Worldline2=1, the output is „AND" operation of Bitline1 and Bitline2.

The schematic and layout of Dual Port SRAM is shown below.

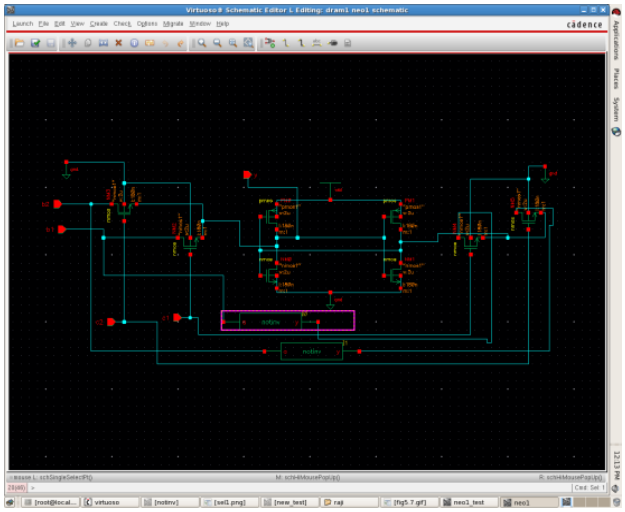

Fig. 6 Schematic Dual Port SRAM cell.

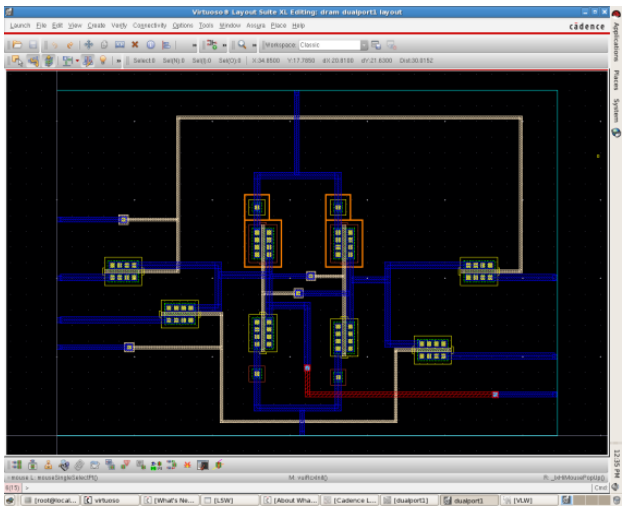

Fig. 7 Layout of Dual Port SRAM cell

b. Applications

1) Embedded use: Many categories of industrial

and scientific subsystems, automotive electronics, and similar, contain static RAM.

2) In computers: The speed and efficiency of Static RAM make it ideal for CPU cache, used to quickly perform calculations.

The cost and space limitations of Static RAM are offset by the relatively small quantities of cache used in modern computers.

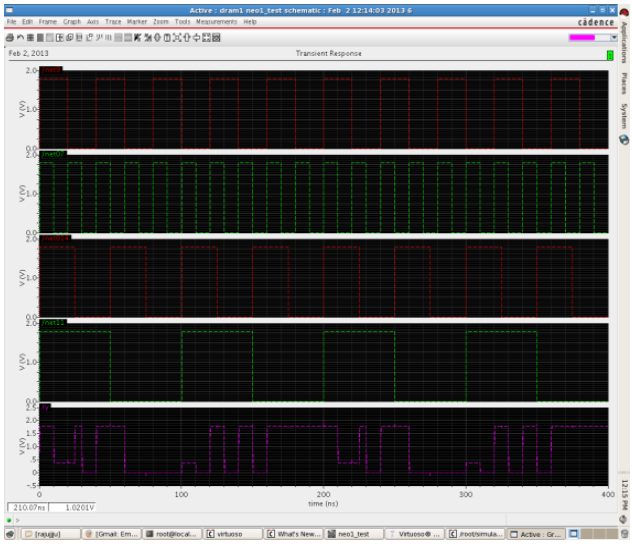

Fig. 8 Write and Read operations of Dual Port SRAM Cell.

Conclusion And Future Scope

a. Conclusion

This chapter discusses the overall contribution of the report. The schematic is designed for storage of 2 bit Memory. The Read and Write operations are observed. The layout for Dual Port SRAM Memory designed. The Dual Port SRAM is capable of storing 2bits.The proposed work is operated with supply voltage 1.8v.The SRAM is designed and implemented in standard GPDK180nm technology using Cadence virtuoso editor for schematic and assura editor for layout.

b. Future work

1) The design in this dissertation can be upgraded to give better performance.

2) Memory size can be increased in order to increase the storage capacity for modern digital applications.

3) Using cadence tool we can write Verilog code in digital labs and can be implemented on hardware.

4) Layout can also be extended up to maximum bits.

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