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Research Article

Design, Simulation and Power Analysis of Sigma-Delta Modulator using 0.18µm CMOS Technology

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Abstract

This paper presents the design technique for a sigma-delta modulator in a standard 0.18µm CMOS technology. This circuitry performs the function of an analog-to-digital converter. A first-order 1-bit sigma-delta (Σ-Δ) modulator is designed, simulated and tested using Cadence 0.18 µm CMOS process technology with power supply of 1.8 V through Cadence. The modulator is proved to be robustness, the high performance in stability .The simulation are compared with those from a traditional analog-to-digital converter to prove that sigma-delta is performing better with low power and area.

Keywords*: Sigma delta (ΣΔ) modulator, Cadence Virtuoso Suite Tool, DRC (Design Rule Check), ERC (Electrical Rule Check), LVS (Layout Versus Schematic) and RCX (Resistor Capacitor extract), Layout area, dynamic power and total power.*

1. Introduction

Advancement in VLSI technology, has allowed a phenomenal growth of the silicon integrated circuits. As there is a remarkable progress in the fabrication, the MOS transistors have been scaled down (T. Shibata et al, 1992). According to Moore's prediction in 1965, the total number of devices on a chip double every 12 months. An Analog-to-Digital converter is a device, which translates an analog voltage signal into a corresponding digital number. Whenever we relate to the real world most of the signals are analog in nature. But some applications such as digital signal processing requires signals to be digital. In such situations it becomes necessary to get analog to digital conversion using an ADC. Analog-to-digital converter (ADC) is a fundamental block in mixed-signal VLSI circuits. The (T. Shibata et al, 1992) rapid growth of mobile electronic systems increases the demand for developing low-cost and low-power circuit technique with high performance. An essential building block of such systems is the analog-to-digital converter (ADC). Sigma delta (ΣΔ) modulators are one of the preferred architectures for high resolution converters. Power consumption and area are the key parameters for a sigma-delta modulator these parameters cannot be changed once an ADC is designed. While it can operate at higher speed and will consume less power when operating at a lower resolution. Such features are highly desirable in many wireless and mobile applications. For example, the strength of a radio frequency (RF) signal varies greatly depending on geographic location. Recently in many wireless mobile applications demand very high speed data converters with wide bandwidth, higher signal to noise ratio and variable (adaptive) resolution with optimized power and cost effectiveness. So there is a need for upgrading the performance of data converters to meet the demands of emerging technologies. So it is a challenging issue in the mixed signal design to have high speed, variable resolution data converters with less space and low power consumption (Aria Eshraghi et al 2004).

2. Topology Sigma Delta Architecture

The block diagram of a first order sigma delta modulator is shown in Fig.1, which consists of a integrator, a comparator, which acts as an ADC and 1-bit DAC, which is placed in the feedback loop. The name first order is derived from the information that there is only one integrator in the circuit, placed in the forward path. When the output of the integrator is positive, the comparator feeds back a positive reference signal that is subtracted

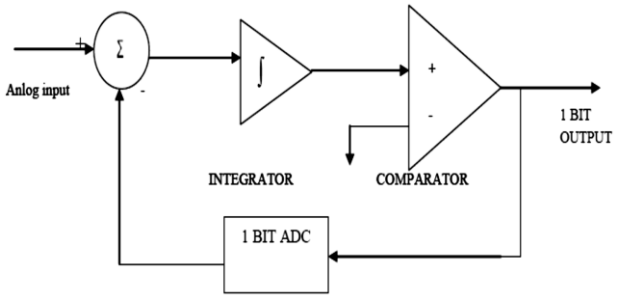

Fig 1: 1 bit Sigma-delta Modulator

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from the input signal of the integrator. Similarly, when the integrator output is negative, the comparator feeds back a negative signal that is added to the incoming signal. The integrator therefore accumulates the difference between the input and quantized output signals from the DAC output which is in feedback loop and makes the integrator output around zero. A zero integerator output implies that the difference between the input signal and the quantized output is zero.

ΣΔ modulation has become popular for achieving high resolution. A significant advantage of the method is that analog signals are converted using not only simple and high-tolerance analog circuits but also analog signal processing circuits having a precision that is usually much less than the resolution of the overall converter. Conventional converters are often difficult to implement in fine-line VLSI technology with reasonably low power consumption. These difficulties arise because conventional methods need analog components that are precise and highly immune to noise and interference. However, the conversion rate of conventional converters is Nyquist rate, i.e. sampling frequency is twice the signal bandwidth. That is why conventional converters are usually referred to as Nyquist converters.

3. Poblem Statement

The goal of this proposed method is design, implementation and layout of 1-bits ΣΔ modulation, according to the following specifications:

- Input voltage range will be 0 to 1.8V and supply voltage will be 2.5 V.
- Resolution will be 1-bits; with area-
- Technology used is 0.18µm
- Tool used to perform this design is Cadence Virtuoso Suite Tool.

4. Methodology

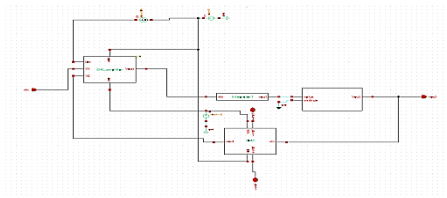

Fig 2: Complete 1-bit sigma delta modulator schematic design

Designing of 1-bit sigma delta modulator has some rules such as

1. Designing of differential amplifier is done by choosing polyresistors from gpdk180 libraries of value 1K, whose length is 79µm and width is 600ηm.
2. Designing of integrator polyresistor and nmoscap (nmos capacitor) from gpdk180 libraries with value of 1k and 0.01pf respectively.
3. The designing of comparator, which compares V_{ref} and V_{in} values and gives digital output in terms of logic "1" and logic "0".
4. Designing of 1 bit DAC (digital to analog converter) as a negative feedback loop.
5. Designing Layout for all schematic circuits.
6. Calculating power consumed and layout area.

4.1 Schematic and Layout Designs of Components

Each component a complete schematic view is designed using MOS transistors and tested with supply voltage of 1.8V. Layout of each component is designed with physical testing of DRC (Design Rule Check), ERC (Electrical Rule Check), LVS (Layout Versus Schematic) and RCX (Resistor Capacitor extract).

4.1.1 Differential amplifier design

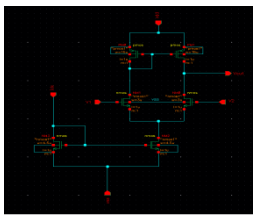

Fig 3: schematic view of differential amplifier

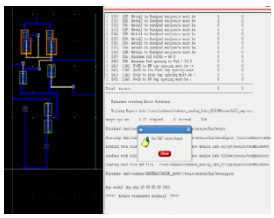

Fig 4: Layout of different--ial amplifier with Assura DRC

4.1.2 Integrator

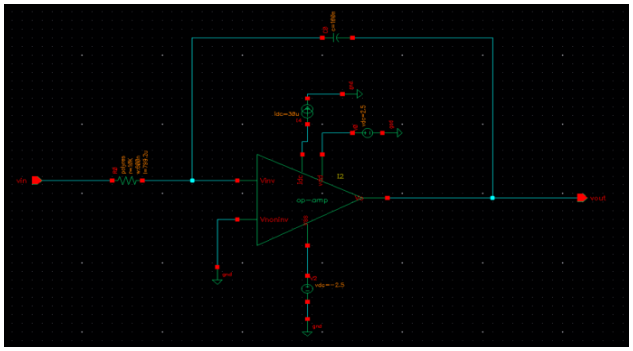

Fig 5: Schematic view of Integrator

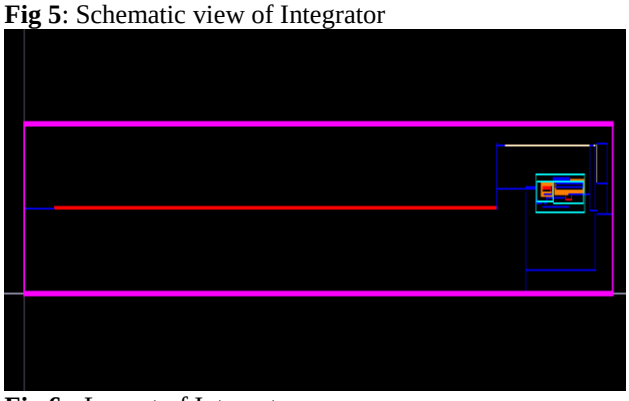

Fig 6: Layout of Integrator

4.1.3 Comparator

If the integrator output is positive, the first comparator will output a "high" signal i.e '1' otherwise "low" i.e '0' which is 1-bit output of the sigma-delta modulator.

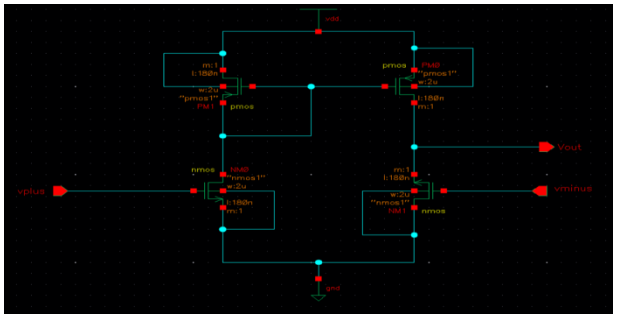

Fig 7: Schematic view of Comparator

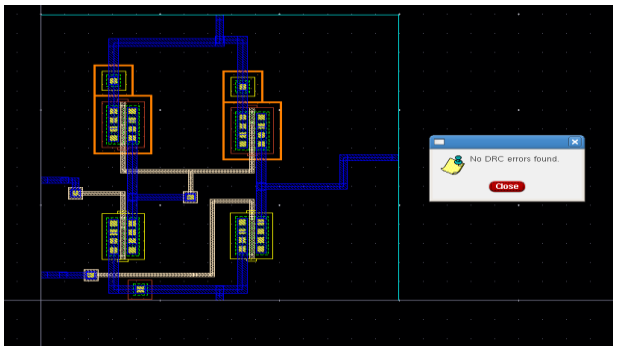

Fig 8: Layout of Comparator with Assura DRC

4.1.4 1 bit DAC

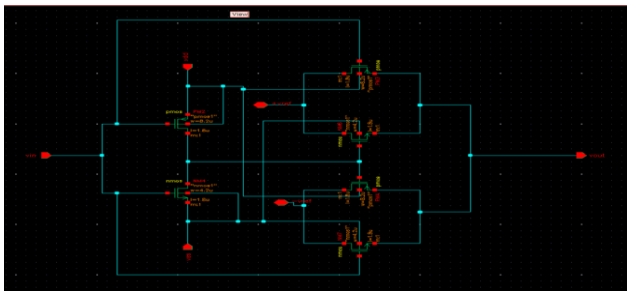

Fig 9: Schematic view of DAC

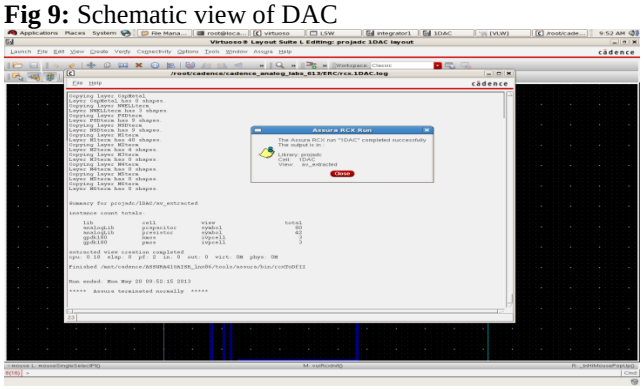

Fig 10: Layout of DAC with Assura DRC

Table 1: AV_extracted results and area

Components	No. of capacitors	No. of resistors	No. of nmos	No. of pmos	Layout Area (in m^2)
Differential Amplifier	91	32	4	2	0.5964e-9
Integrator	41	36	4	3	8.7995e-8
Comparator	32	13	2	2	2.2537e-10
1 bit DAC	80	42	3	3	4.4e-9

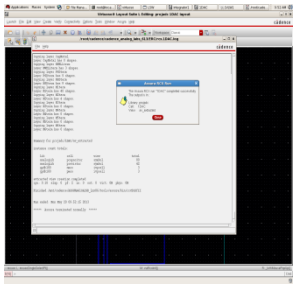

Fig 11: RCX of DAC

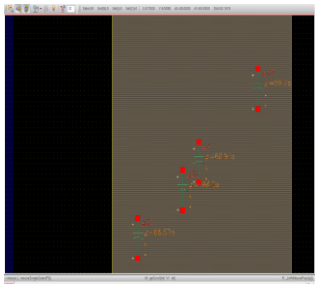

Fig 12: DAC av_extract

5. Results

Sigma delta modulator produces output with 1 bit resolution with reference voltage of 2.5 V from the comparator .If the voltage is higher than the reference voltage its high i.e '1' if it is lower than the reference voltage it is low i.e '0'as show in the figure12. The dynamic power consumed by sigma delta modulator is 9.284e-3w with total power 8.376e-3.

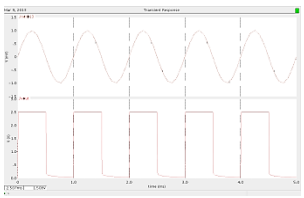

Fig 13: 1- Bit Sigma delta output

Conclusion

As the cadence analog tool deals with the analog environment with 0.18um CMOS technology. In this way we have developed a Sigma-Delta modulator, which converts an analog input into a digital if the above specifications satisfied. This can be used in application of ADC having 2MHz frequency can be used in various audio, communications, data acquisition systems and DSP (Digital Signal Processing) applications. It gives low power system that is the need of today's world.

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