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Research Article

Applying Shannon Expansion Concept for Power Optimization of Digital design

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Abstract

Power dissipation is one of the biggest challenges and is the main concern in VLSI systems. In this paper, a new style of logic design based on Shannon's decomposition theorem is used to reduce the power consumption. The paper considers various types of designs using Shannon's expansion theorem to reduce the power consumption in digital system and a design that enables to achieve substantial reduction in power consumption is developed. The concept is been applied to the multiple digital circuits. And it is proved that the proposed concept have major power reduction when the system is complex. Almost 40% of power reduction was achieved when applied to 128:1 MUX. The design is simulated using Xilinx. The circuit synthesizability is verified using RTL compiler of Cadence. The synthesis reports are compared to arrive at a conclusion. This concept can easily be applied even to Design for testability [DFT], especially during Scan test where there is big requirement of power reduction.

Keywords*: Verilog, Xilinx, Shannon's expansion theorem, RTL complier, Design for Testability [DFT]*

Introduction

Power optimization of Digital Design

The basic concern in the VLSI system is the power, area and speed. As the technology shrinks, it becomes portable and it uses battery operated systems. At the same time due to large packing density, its total power dissipation also increases. Power is the main concern in today's scenario, due to smaller feature size in scale down technology the aggregate switching power increases from one technology generation to next. So, the dynamic power consumption affects the battery life of the devices such as mobile phones, iPods, tablets etc.

Power dissipation in the VLSI circuit is mainly due to static power, short circuit power and dynamic power. Dynamic power plays dominant role in power dissipation of the circuits. The dynamic power dissipation is due to charging and discharging of the capacitors. As the system complexity increases, due to switching activity the dynamic power dissipation also increases . Many efforts are made in this direction and the results showed that significant power reduction can be achieved, however these efforts are from analog approach and the circuits become complex. The discussion holds good even in test mode of device operation. The power reduction in testing is crucial. In test mode major power dissipates when compared with normal mode because in test mode all gates will be active results in higher power dissipation. It will be almost more than 60% to 70% in scan-based testing. Hence, it is important to consider the problems related to power dissipation in the digital design implementation considering also the low power testability. The design based on Shannon concept is very useful in reducing the test power in digital design. The Shannon based design implementation have multiple advantages. The scan register and test application procedure can be easily performed without any alterations. Even At-speed testing is possible with no changes.

In this paper, the Shannon's expansion theorem is used to reduce the power dissipation in the circuit part. The proposed method is implemented using digital approach using Verilog simulated to ensure the logic and synthesized to compare the reports obtained.

Shannon's expansion concept for Low power design

Shannon's expansion is used to reduce the power consumption. It apportions the Boolean expression into two sub expressions as shown below.

Shannon expansion Concept

$$f(x_1,..x_i,..x_n) = x_i \cdot f(x_1,..,x_i=1,..x_n) + x_i' \cdot f(x_1,..x_i=0,..,x_n) \quad (1)$$

$$= x_i CF_1 + x_i' CF_2 \quad (2)$$

where $CF_1 = f(x_1,..,x_i=1,..x_n)$, $CF_2 = f(x_1,..x_i=0,..,x_n)$

Where, x_i is the control variable, and CF_1 and CF_2 are called cofactors. From the above expression it is clear that depending on the state of the control variable (x_i), the

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computed output of only one of the cofactors (CF_1 or CF_2) is considered at any given instant of time. The output of CF_1 and CF_2 are combined using a multiplexer (MUX), which is controlled by x_i .

Control variable selection for partitioning is required to be done to balance the resulting cofactors. Balancing of cofactors ensures that the circuit exhibits a similar amount of static current for any test vector. It can be illustrated using the conventional multiplexer as shown in the Fig 1 it uses entire design to get the output. The usage of Shannon's expansion in this scenario leads to low power consumption. To prove the above concept simplest digital circuits have been considered. The conventional digital design implementation is shown in Fig 1.

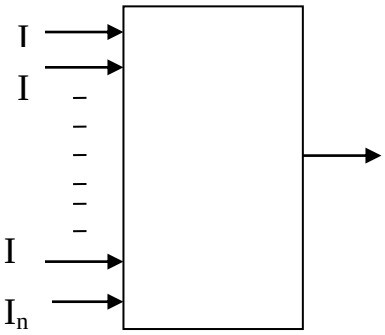

Fig 1. Conventional implementation of digital design

In Shannon's expansion at any instant of time only a part of the digital design is been considered to get the output i.e Cofactor -1 if x_i is zero and Cofactor -2 if x_i is one as shown in Fig 2.

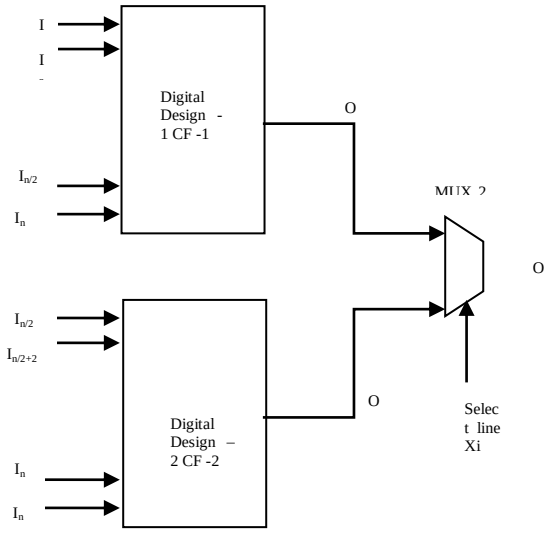

Fig 2 Implementation of digital design based on Shannon expansion

The system uses multiplexer at the end to choose the true or complementary input. Depending on the select signal, the upper part or lower part of the circuit is active and the other part is completely switched off. According to Shannon only half of the terms are used at a time when compared to conventional design which uses all terms. Due to part of the circuit is active at a time of switching in the circuit the dynamic power consumed reduces and in turn reduces the total power

Results and discussions

In order to prove the concept multiplexer with different ratios have been considered. The conventional digital design implementation and Shannon based are coded in Verilog and simulated to ensure the logic using ncsim from Cadence. The synthesis report is obtained from RTL Complier from Cadence. The schematic obtained for 8:1 Mux for conventional is shown in Fig 3. It can be seen from the Fig 3 that for any combination of input, the entire design will be activated which leads to unnecessary switching of the gates leads to large power consumption.

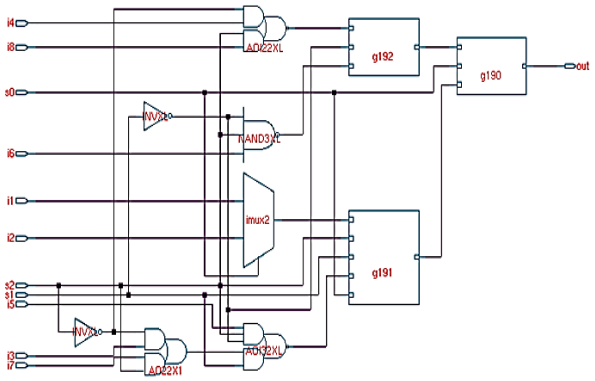

Fig 3. Schematic of conventional 8:1 multiplexer

In case of Shannon expansion part of the circuit is used. In this context, two functions are used to implement the required circuit i.e. true and complementary functions for 8:1 multiplexer, if S0,S1 and S2 are the select signals and I1 to I8 are the input signals then using Shannon expansion ,

$$Out = S_0' (S_1'S_2'I_1 + S_1'S_2I_2 + S_1S_2'I_3 + S_1S_2I_4) + S_0 (S_1'S_2'I_5 + S_1'S_2I_6 + S_1S_2'I_7 + S_1S_2I_8) \quad (3)$$

Depending on the select signal S_0, true or complementary functions are used to get the output. According to Shannon, only four terms are used at a time when compared to conventional design which uses 8 terms. Since only a part of the circuit is active at a any instance of time. The switching of the gates reduces and hence dynamic power. Conventional multiplexer consumes more power when compared to proposed method due to large switching activities. Using Shannon expansion theorem part of the switching activity is reduced so power consumption is also reduced as shown in the Fig 4.

In this paper many designs are implemented to check the power consumption. Table 1 shows the power consumption of various circuits and comparison of conventional method and proposed Shannon based method. The reports were generated for different configuration and compared to arrive at a conclusion. The consolidated synthesis report obtained for digital design

from cadence RTL Complier power is given in Table 1. Power analysis plot based on the synthesis report for conventional design and Shannon based circuit is shown in Fig 5.

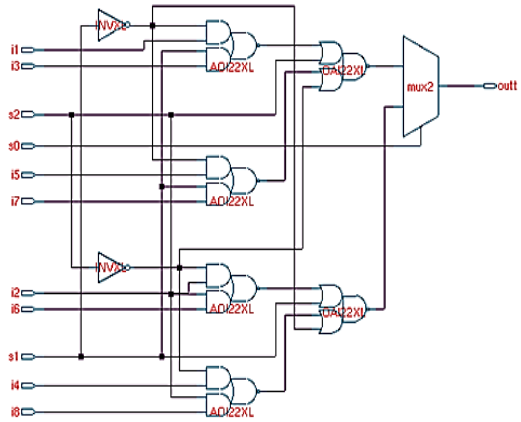

Fig 4. Schematic of Shannon based 8:1 multiplexer

Table 1. Power comparison of various multiplexers

Design	Conventional Approach in nW			Shannon based Approach in nW			Difference in nW
	Leakage	Dynamic	Total	Leakage	Dynamic	Total	
8:1 MUX	86.418	676.57	762.99	75.991	653.17	729.1	33.901
16:1 MUX	153.11	1553	1747.1	158.55	1506.6	1706.1	40.991
32:1 MUX	315.93	2352.5	2668.4	307.37	2308.3	2615.7	53.578
64:1 MUX	494.62	4417.9	4912.5	597.38	4067.5	4646.9	265.61
128:1 MUX	1007.9	6690.9	7698.8	539.31	4070.2	4609.5	3089.3

Power consumption is more in case of conventional method for complex circuits when compared with Shannon expansion based design which is depicted in Fig 5. The power reduction varies from 5% to 40% based on the complexity involved in the design.

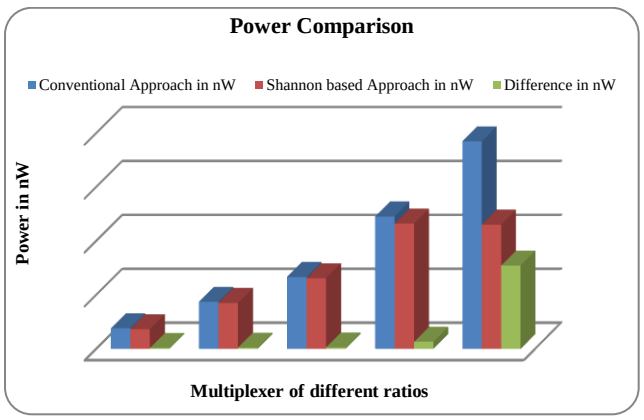

Fig 5. Comparison of conventional design with Shannon based design.

Conclusion

Power reduction is the significant step in the battery operated portable devices in the VLSI system. Power reduction is the need of the day, to do so in this paper Shannon expansion theorem is used and compared with conventional approach. The Proposed method gave promising power reduction of 40% to 128:1 MUX. Without any doubt when this method is applied to complex design the power reduction will be large i.e. as the design becomes more complex power reduction will be more. This low power technique finds importance in testing methodology where it has become mandatory.

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