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Research Article

Simulation and Modeling of OFDM Systems and Implementation on FPGA

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Abstract

This paper presents the design and implementation of Orthogonal Frequency Division Multiplexing(OFDM) transmitter and receiver on Field Programmable Gate Array(FPGA). Orthogonal Frequency Division Multiplexing (OFDM) is a multi-carrier modulation technique which divides the available spectrum into many carriers.The bit error ratio with Quadrature Amplitude Modulation for OFDM using Matlab7.8.0® simulation is presented. Bit Error Ratio(BER) performance varies between 10^{-2} to 10^{-3}.The OFDM system is synthesized using Verilog HDL and Modelsim 6.2C.Implementation is done using Xilinx Spartan 3an FPGA board.

Keywords: *OFDM, FPGA, BER Simulation, Verilog HDL,Modelsim6.2C*

1. Introduction

[1]Orthogonal frequency division multiplexing is a multicarrier transmission system in parallel. This parallel transmission greatly expands the pulse length and increase the performance of anti-multipath fading. Its biggest feature is the high data transfer rate with a strong anti channel interference and the channel selective fading capacity. Although OFDM was first developed in the 1960s, only in recent years, it has been recognized as an outstanding method for high-speed cellular data communication where its implementation relies on very high-speed digital signal processing.

OFDM divides the available spectrum into a number of overlapping but orthogonal narrowband subchannels, and hence converts a frequency selective channel into a nonfrequency selective channel . Moreover, ISI is avoided by the use of CP, which is achieved by extending an OFDM symbol with some portion of its head or tail [9]. With these vital advantages, OFDM has been adopted by many wireless standards such as DAB, DVB, WLAN, and WMAN [10,11].OFDM has been widely used in IEEE 802.11a protocol, Asymmetric digital subscriber loop(ADSL), Digital audio broadcasting(DAB), Digital video broadcasting(DVB), High definition TV and so on.

This paper is organized as follows: Section 2 provides principles of OFDM and its Modulation schemes. Section 3 contains OFDM Transmitter and Receiver architectures. Section 4 deals with the issues related to memory based FFT processor. Section 5 gives BER Simulation results and some examples of OFDM.

2. Theory of ofdm

An OFDM system is able to achieve higher and reliable data rates, transmit symbols at at lower rate, and transmit more symbols in parallel streams. Since OFDM utilizes several parallel sub-carriers at the same time, it is able to recover from errors more efficiently, as not all of the information can be impacted from interference sources. The translates into higher and sustainable throughput specifically in locations where non-line-of-sight(NLOS) conditions exist.

In a conventional serial data system, the symbols are transmitted sequentially, with the frequency spectrum of each data symbol allowed to occupy the entire available bandwidth. In a parallel data transmission system several symbols are transmitted at the same time, OFDM can be imply defined as a form of multicarrier modulation . where its carrier spacing is carefully selected so that each subcarrier is orthogonal to the other subcarriers.

In a normal Frequency Division Multiplexing system, the many carriers are spaced apart in such way that the signals can be received using conventional filters and demodulators. In such receivers, guard bands have to be introduced between the different carriers and the introduction of these guard bands in the frequency domain results in a lowering of the spectrum efficiency.

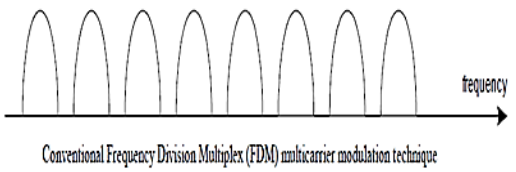

Fig 1. Conventional Frequency division multiplex(FDM) Multicarrrier modulation technique

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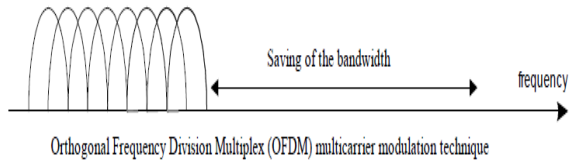

Fig 2. Orthogonal frequency division multiplex(FDM) Multicarrier modulation technique

2.1. Orthogonality Principle

It is possible to arrange the carriers in an OFDM signal so that the sidebands of the individual carriers overlap and the signals can still be received without adjacent carrier interference. In order to do this the carriers must be mathematically orthogonal . The 'Orthogonal' part of the OFDM name indicates that there is a precise mathematical relationship between the frequencies of the carriers in the system. Two periodic signals are orthogonal when the integral of their product over one period is equal to zero.

For the case of continuous time:

$$\int_0^T \cos(2\pi n f_0 t)\cos(2\pi m f_0 t)\,dt = 0, (m \neq n)$$

For the case of discrete time:

$$\sum_{k=0}^{N-1} cos\left(\frac{2\pi kn}{N}\right) cos\left(\frac{2\pi km}{N}\right) dt = 0, (m \neq n)$$

To maintain orthogonality between sub-carriers, it is necessary to ensure that the symbol time contains one or more multiple cycles of each sinusoidal carrier waveform. In the case of OFDM, the sinusoids of our sub-carriers will satisfy this requirement since each is a multiple of a fundamental frequency. Orthogonality is critical since it prevents inter-carrier interference. ICI occurs when the integral of the carrier products are no longer zero over the integration period, so signal components from one sub-carrier causes interference to neighboring sub-carriers. As such, OFDM is highly sensitive to frequency dispersion caused by Doppler shifts, which results in loss of orthogonality between sub-carriers.

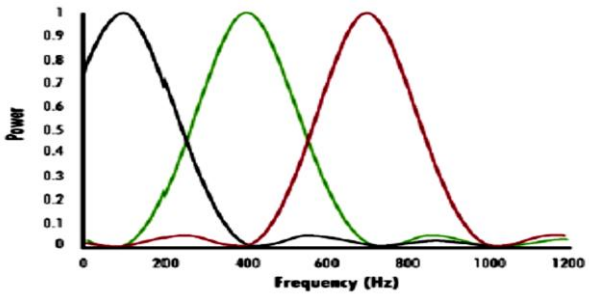

Fig 3. Orthogonality of Subcarriers

2.2. Modulation scheme

The Modulation method of each carrier in OFDM may be different and each carrier can adopt different Modulation methods such as BPSK,QPSK,FPSK,16 QAM,64 QAM,etc . According to the channel conditions to get the best balance between frequency spectrum utilization and bit error rate(BER).We Simulated our results for 16 QAM and 64 QAM.

Quadrature Amplitude Modulation (QAM) is a modulation scheme in which two sinusoidal carriers, one exactly 90 degrees out of phase with respect to the other, are used to transmit data over a given physical channel. Because the orthogonal carriers occupy the same frequency band and differ by a 90 degree phase shift, each can be modulated independently, transmitted over the same frequency band, and separated by demodulation at the receiver. For a given available bandwidth, QAM enables data transmission at twice the rate of standard pulse amplitude modulation.

A broad class of digitally-modulated carrier signals $C(t)$ can be expressed in double sideband suppressed carrier Quadrature component notation as

$$C(t) = I(t)\cos w_c t + Q(t)\sin w_c t \qquad (3)$$

where $I(t)$ and $Q(t)$ are the in-phase and Quadrature phase modulator base band signal sequences, respectively. In the case of QAM, $I(t)$ and $Q(t)$ are the pulse sequences whose amplitudes are data-dependent. The incoming serial binary data stream $d(t)$ is split into two binary parallel branches to constitute the $I(t)$ and $Q(t)$ symbol streams.

3. Design and implementation of OFDM system

3.1.OFDM Transmitter design

The architecture of proposed OFDM transmitter is shown in fig 4. The control unit synchronizes the operation all the blocks in order to avoid any timing mismatches.

OFDM transmitter gets its input a serial bit of information and it is converted to parallel data of four bits. These parallel data is given as input to 16-QAM Mapper which will generate In-phase (I) and Quadrature(Q) components according to constellation diagram.

Symbol generator module is used for generating symbols which will given to zero padding .Here one symbol means set of In-phase and Quadrature components. In this design, symbol generator can store four symbols and will outputted to zero padding module at a time.

Zero padding mainly used for time and frequency synchronization. For making the system robust zero padding can be add before the IFFT.Here zeros are appending before and after the symbols coming from the symbol generator module ,so that output of zero padder is eight symbols which will given as input to 8-point IFFT processor.

The IFFT transform a spectrum (amplitude and phase of each component) into a time domain signal. It converts a number of complex data points into the same number of points in time domain.

The output from the IFFT is given to cyclic prefix adder module by serially. The Cyclic Prefix is a copy of the last three samples from the IFFT, which are placed at the beginning of the OFDM symbol.

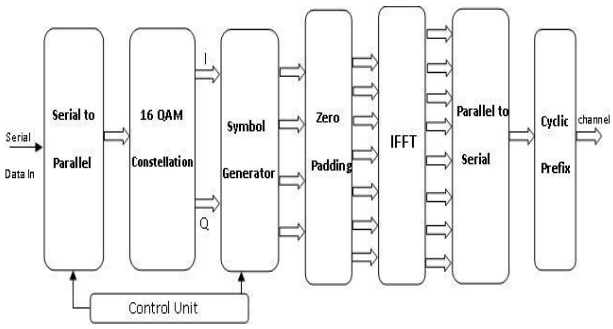

Fig 4. Architecture of Proposed OFDM Transmitter

3.2. OFDM Receiver design

Fig 5 shows the architecture of proposed OFDM receiver The cyclic prefix was added at the transmitting end in order to avoid inter-symbol interference, therefore during reception it must be eliminated for any further processing of the received signal . This is done by simply skipping the first three samples in the received OFDM symbol. The control unit synchronizes the operation all the blocks in order to avoid any timing mismatches. Demodulation can be made by FFT which requires parallel data, so serial to parallel converter take care of that parallel conversion. Zeros which are appended at the transmitter should be removed before giving to 16-QAM constellation de mapper.The function of the symbol divider is to handle four symbols and will give one symbol to the QAM de-mapper. Here one symbol means set of In-phase and Quadrature components. By getting I and Q values from the symbol divider ,QAM de-mapper gives back four bits of information using constellation diagram. These parallel bits of information will convert to serially to retrieve transmitted bits.

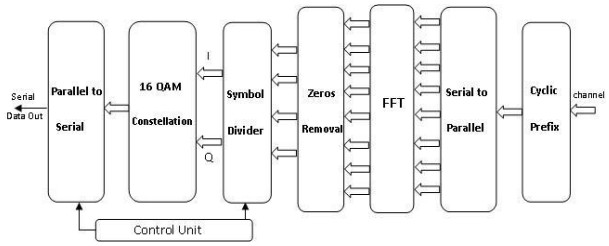

Fig 5. Architecture of Proposed OFDM Receiver

4. Memory based FFT processor

Fig.6 shows the block diagram of an efficient FFT processor for OFDM systems . For simplicity of design, we divide the FFT processor into several functional units: butterfly unit, data address generation, twiddle address generation, timing control, data switch, and block float-point unit. Some memory units are also required: RAM1, RAM2, RAM3, RAM4 and ROM. The function description of each unit is listed below:

(1) Butterfly unit: the kernel of FFT processor, conduct the 4- point DFT and multiplications with twiddles;
(2) Data address generation: generate the address for reading data and writing data;
(3) Twiddle address generation: generate the address of twiddle factor coefficients (for simplicity of description, we call it twiddle at the rest of the paper) for radix-4 butterfly operation;
(4) Data switch: conduct the switch between RAMs;
(5) Block float-point unit: Conduct block float-point operation: collect the bit length information of the data out of butterfly and truncate it to the length required;
(6) Timing control: Control the timing of all the other units;
(7) RAM1 and RAM2: store the input data and internal data;
(8) RAM3 and RAM4: store the output data and internal data. Butterfly unit area is 80% of FFT processor, and its speed decides the speed of FFT processor. So, it is very important to develop the processing speed of butterfly and reduce its areas simultaneously. In the proposed architecture, radix-4 butterfly unit for decimation-in-frequency (DIF) FFT is considered. It is the core of the FFT processor, and performs radix-4 butterfly operation. In order to meet the requirement of high-speed data transmission and low-area consumption in OFDM systems, two novel butterfly algorithms -- parallel butterfly algorithm and dual butterfly algorithm are proposed in the article, which will be described in the next two sections.

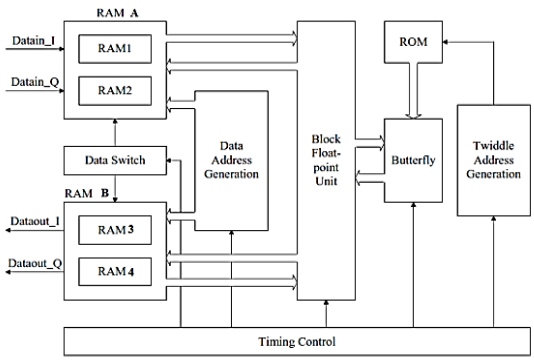

Fig 6. Memory Based FFT Processor

5. Simulation results

Matlab 7.8.0 is a high level computing Language and Interactive Environment used for data Visualisation,data analysis and numerical calculation .In this paper Matlab GUI is used to create Simulation model.Fig 5. Shows the BER for 96 Input carriers.Similarly for 120,140 and 160 input carriers is shown in Table I.Fig 7 shows the Bit Error Ratio as a Function of Signal to Noise ratio.(SNR)

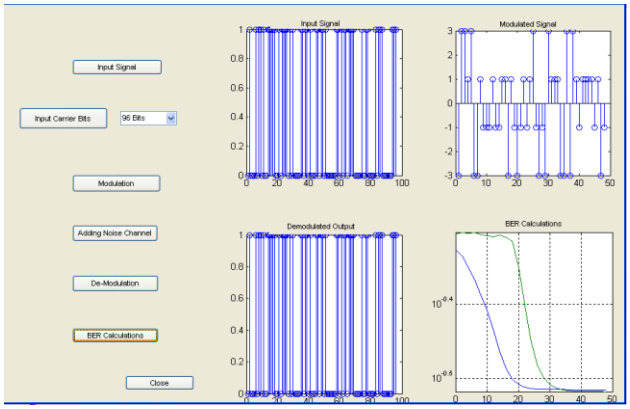

Fig 7. Graphic user interface

Table I. Results for BER and SNR of 16 QAM and 64 QAM

	Bit Error Ratio (BER)	Signal to Noise Ratio (SNR)
INPUT CARRIERS:96		
16QAM	$10^{-0.34}$	47db
64QAM	$10^{-0.30}$	48db
INPUT CARRIERS:120		
16QAM	$10^{-0.298}$	48db
64QAM	$10^{-0.300}$	48db
INPUT CARRIERS:140		
16QAM	$10^{-0.3}$	48db
64QAM	$10^{-0.302}$	48db
INPUT CARRIERS:160		
16QAM	$10^{-0.302}$	48db
64QAM	$10^{-0.296}$	48db

The Bit error ratio(BER) performance varies between $10^{-0.2}$ to $10^{-0.3}$.

5.1.OFDM Transmitter

We have used verilog Tool, Verilog is based on C. Verilog is easier to learn and has very simple data types. The Verilog language was originally developed with gate level modeling in mind, and so has very good constructs for modeling at this level and for modeling the cell primitives of ASIC and FPGA libraries.

Hence we have presented an example shown in Table II for Transmitter.

Table II. Example for OFDM Transmitter

Input	Output
x0 = 0 + 0i	x(0) = 2.5298
x1 = 0 + 0i	x(1) = -2.60633 – 0.18533i
x2 = 0.31622 + 0.31622i	x(2) = 1.26492 + 1.26492i
x3 = 0.31622 + 0.31622i	x(3) = -0.18533 – 2.60633i
x4 = 0.94868 + 0.94868i	x(4) = 2.5298
x5 = 0.94868 - 0.94868i	x(5) = 0.07653 – 1.07959i
x6 = 0 + 0i	x(6) = 0
x7 = 0 + 0i	x(7) = -1.07959 + 0.07959i

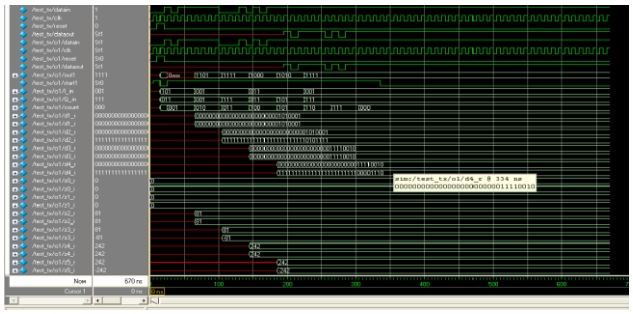

Fig 8. Simulated waveforms for ofdm transmitter

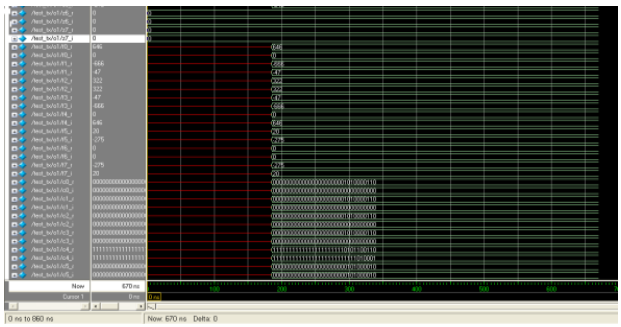

Fig 9. Simulated waveforms for ofdm transmitter

5.2.OFDM Receiver

In this the transmitted bits are received at the receiver section. The example is presented in table III for Receiver.

Table III. Example for OFDM Receiver

Input	Output
x(0) = 2.5298	x0 = 0 + 0i
x(1) = -2.60633 – 0.18533i	x1 = 0 + 0i
x(2) = 1.26492 + 1.26492i	x2 = 0.31622 + 0.31622i
x(3) = -0.18533 – 2.60633i	x3 = 0.31622 + 0.31622i
x(4) = 2.5298	x4 = 0.94868 + 0.94868i
x(5) = 0.07653 – 1.07959i	x5 = 0.94868 - 0.94868i
x(6) = 0	x6 = 0 + 0i
x(7) = -1.07959 + 0.07959i	x7 = 0 + 0i

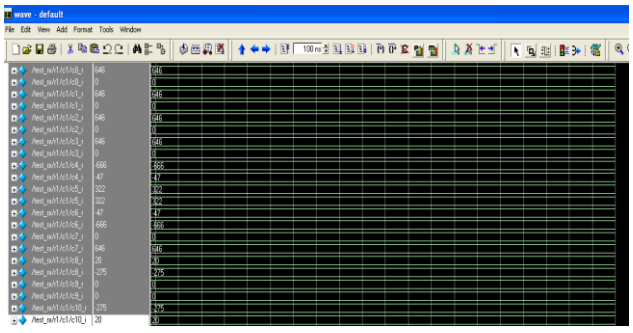

Fig 10. Simulated waveforms for OFDM receiver

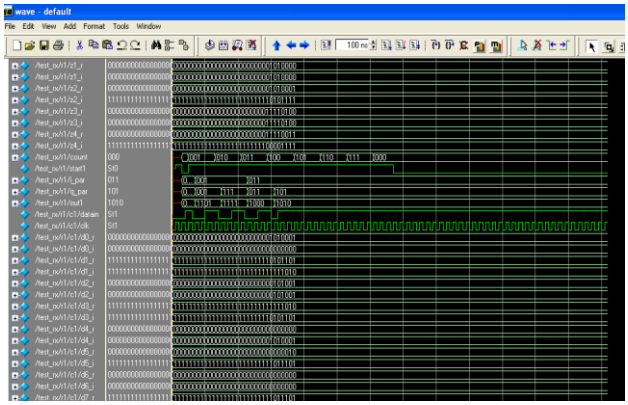

Fig 11. Simulated waveforms for ofdm receiver

The verilog code for FFT and IFFT processor is synthesized using Xilinix ISE 10.1 and gate level netlist is obtained. From this bit file is generated and downloaded it to Spartan 3an FPGA.

6. Conclusion

We conclude that the design and implementation of orthogonal frequency division multiplexing(OFDM) transmitter and receiver on FPGA.The bit error ratio with quadrature amplitude modulation for OFDM using matlab simulation is presented. The BER performance varies between $10^{-0.2}$ to $10^{-0.3}$ and the transmitted bits is received at the receiver section. Finally the OFDM system is synthesized using Verilog HDL and Modelsim 6.2C.Implementation is done using Xilinx Spartan 3an FPGA board. The good capability of the OFDM design and implementation promises a bright future of OFDM.

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