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Research Article

Implementation of an Efficient OFDM transmitter and Receiver Using FPGA

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Abstract

In this paper an efficient implementation of an Orthogonal Frequency Division Multiplexing (OFDM) system is proposed. Nowadays a lot of researches are going on OFDM since it is a high speed modulation technique and can be used in optical fiber communication systems. Also OFDM utilizes the available bandwidth with maximum efficiency. The proposed architecture improved the efficiency of the system by improving the error detection and correction method. The proposed method saves a considerable amount of time when an error occurs in the transmitted data and the system demands retransmission. The proposed system is simulated using Xilinx ISE 14.2 and successfully implemented on Spartan 6 FPGA.

Keywords: *Orthogonal Frequency Division Multiplier, Modulation, Optical fiber communication.*

1. Introduction

Nowadays OFDM is considered as an emerging modulation technique for the modern communication systems. The modern system demands efficiency as well as high speed. Even if the speed of the system is very high, if the system fails to provide the required efficiency then it will became a waste product. There comes the importance of the OFDM with error detection and correction.

OFDM is becoming widely applied in wireless communications systems due to its high rate transmission capability with high bandwidth efficiency and its robustness with regard to multipath fading and delay (Reza Ghanaatian *et al*., 2014). Researches are going on to fit it to the optical fiber technology. Also inexpensive and high performance CMOS chipsets based on OFDM techniques are entering the market which in turn increases the demand of OFDM.

OFDM is a multicarrier modulation technique in which the carriers are orthogonal to each other. Due to this the guard bands can be eliminated in the OFDM system thus reducing the required bandwidth for a specified data bits. Also it reduces the Inter Symbol Interference (ISI).

2. Related Works

OFDM is a wideband wireless digital communication technique that is based on block modulation. These blocks may contain one or more symbols. Symbols are modulated using subcarriers. These subcarriers are arranged in such a way that they do not overlap each other and maintains orthogonality. The OFDM is very effective in reducing the ISI and handling the multipath fading in the communication channels.

R.W. Chang proposed the principals of OFDM in the year 1966 (R.W. Chang., 1966) and achieved a patent for the same in the year 1970. In his design the crosstalk was a severe problem. Also the system became quite complex when a large number of subcarriers are needed.

In 1971 Ebert and Weinstein proposed a modification to the system. They used the DFT (Discrete Fourier Transform) to produce the orthogonal subcarriers (Weinstein *et al*., 1971) and there by reduced the complexity of the system considerably. But later this was replaced with FFT (Fast Fourier Transforms), which is less complex and faster compared to DFT.

In 1980s Peled and Ruiz introduced Cyclic Prefix to the OFDM system in order to reduce Inter Channel Interference (ICI) (Peled *et al*., 1980). Currently this is adapted to the IEEE standards.

From 1990 onwards OFDM system has been exploited for the high data rate communications.

3. OFDM System Description

OFDM is a multi-carrier modulation technique in which the carriers are placed orthogonal to each other. Due to this the Inter Symbol Interference (ISI) is reduced and

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the need for guard bands is eliminated. High spectral efficiency and resistance towards multipath makes OFDM a better choice for wireless communication systems. The OFDM possesses a low bit error rate and high data rate than the conventional system. The block diagram of an OFDM system is shown in figure 1.

1. Scrambler

The scrambler is used for randomizing the data in order to reduce burst errors. It avoids the occurrence of long 1's and 0's in the transmitted data. It reduces the dependence of signal's power spectrum on actual transmitted data. We can use a Pseudo random generator to encrypt the data. So scrambler consists of a number of shift registers with feedback connections.

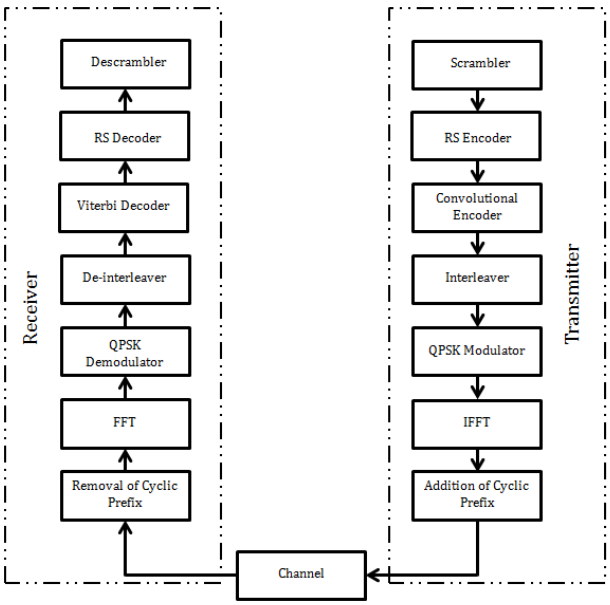

Fig.1 The OFDM system

2. Descrambler

The descrambler circuit is used to retrieve the scrambled data. It consists of a number of feed forward shift registers.

3. Reed Solomon Encoder

Reed Solomon codes are non binary cyclic codes with m bit sequences, where m is greater than 2. For the most conventional RS(n,k) code,

$$n = 2^m - 1 \quad (1)$$
$$k = 2^m - 1 - 2t \quad (2)$$

Where n is the total number of code symbols encoded in the block, k is the number of data signals being encoded and t is the error correcting capability of the code. The number of parity symbols encoded with each block is 2t.

$$2t = n - k \quad (3)$$

4. Reed Solomon Decoder

The RS decoding is done using Petersen–Gorenstein – Zierler (PGZ) algorithm. It consists of five steps.

1. Syndrome calculation
2. Key equation solver
3. Chien search
4. Forney algorithm
5. Error correction

In the first step the syndrome values are calculated in order to find the presence of an error. The 2t syndrome values are calculated from the received data. These values can be calculated by dividing the receiver polynomial with the generator polynomial. If all the syndrome values are zero then the received code word is correct.

In the key equation solver stage the 2t syndrome values are solved in order to find the error locations and error values.

In Chien search the error polynomial is evaluated. The reciprocal of the roots of this polynomial represents the error locations.

In the Forney algorithm the error values are found using the syndrome values and the roots of the error polynomial.

FIFO is used in the end for error correction.

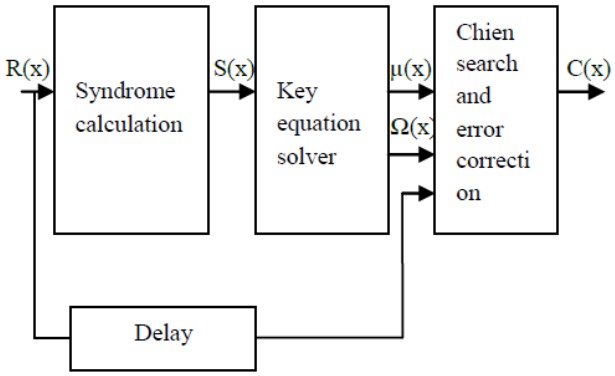

Fig.2 The block diagram of RS Decoder.

5. Convolutional Encoder

It's a Forward Error Correction (FEC) method which is used to correct the errors caused due to the noise in the channel. In the encoder redundant bits are added with the data and send to the receiver. The process of adding redundant data is known as channel coding.

The convolutional encoders are represented using two parameters. The code rate is the m/n ratio where m is the number of bits into the Convolutional encoder and n is the number of output bits. The transformation of m bits to n bits depends on the last k bits. It is known as the constraint length.

6. Viterbi Decoder

The Viterbi decoding can be explained using the trellis diagram.

1) Calculate the Branch metrics
2) Recursively compute the shortest paths to time n, in terms of the shortest paths to the time $n-1$. This is known as add compare and select recursion.
3) Find the shortest paths to each of the trellis states using step 2. This is known as survivor path decoding. After tracking each of the survivor path track the signal path.

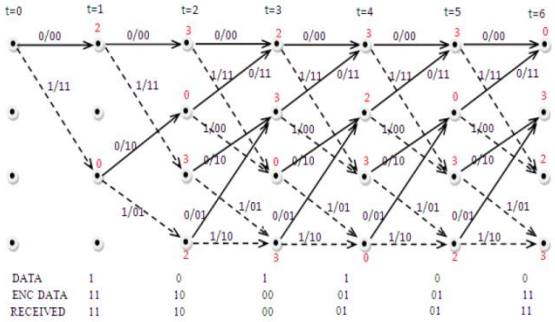

Fig.3 Trellis Diagram

7. Interleaver / Deinterleaver

The interleaver is used to reduce the burst errors. In the interleaver the incoming bits are rearranged so that they are no longer adjacent to each other. In case of OFDM the adjacent bits are rearranged in such a way that they are placed on non adjacent subcarriers. In the receiver end the deinterleaver rearranges the data back into the original form.

8. QPSK (Quadrature Phase Shift Keying) Modulator & Demodulator

Due to its bandwidth conserving property and less complex circuit compared to QAM, (Quadrature Amplitude Modulation) QPSK modulation scheme is used in this paper to modulate and demodulate the subcarriers of the OFDM system.

9. Inverse Fast Fourier Transform (IFFT) / Fast Fourier Transform (FFT)

In OFDM the FFT and IFFT are used to generate the orthogonal subcarriers. IFFT converts the time domain signal into frequency domain. In the receiver the FFT converts the time domain signal back to the frequency domain.

10. Cyclic Prefix

Cyclic guard intervals are introduced into the system in order to preserve the orthogonality and the independence of subsequent symbols. CRC (Cyclic Redundancy Check) is used to generate the guard intervals. The CRC16 is used here. The generator polynomial used is

$$g(x) = x^{16} + x^{12} + x^5 + 1 \quad (4)$$

Here if any error occurs in the system the CRC detects the error and demands the transmitter to resend the data. It will adversely affect the overall speed of the system. In this paper the CRC is modified in such a way that we can detect two bit errors and correct the single bit errors.

Let C_{Tx} is the CRC calculated in the transmitter and C_{Rx} is the CRC calculated in the receiver section. If no errors are occurred during transmission then both the calculated values will remains the same. If they are not equal then there occurs some error in the received data and we need to find the error position. If it is a single bit error we can correct the error. In such cases we will calculate the syndrome value. The syndrome value is given as,

$$Syn = C_{Tx}\ xor\ C_{Rx} \quad (5)$$

There are two cases in which a single bit error can occur. One is the single bit error in the data bits and the second one is a single bit error in the checksum bits. We need to correct only if the error occurs in the data bits. Now an error polynomial is formed which has a coefficient only in the error position. Then the correct data can be obtained by xoring the error polynomial and the syndrome value.

4. Results & Discussions

A. Scrambler & Descrambler

The output waveforms of the scrambler and descrambler are shown in figure 4 and 5 respectively.

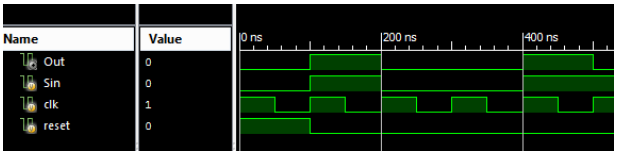

Fig.4 Output waveform of scrambler.

Fig.5 Output waveform of descrambler.

The single bit input given in the scrambler circuit is retrieved using the descrambler.

B. RS Decoder & Encoder

The inputs applied to the RS encoder are 111, 110 and 010. These are encoded using 7 symbols. The output wave of the RS encoder is shown in figure 6.

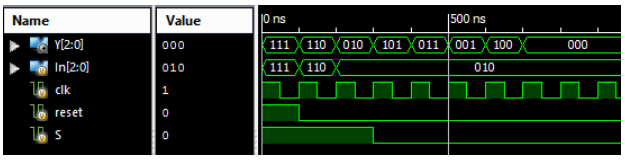

Fig.6 Output waveform of RS encoder

The RS decoder receives the encoded values and retrieves the original value. The output waveform of RS decoder is shown in figure 7.

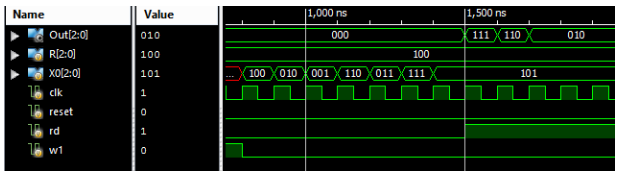

Fig.7 Output waveform of RS decoder

C. Convolutional Encoder & Viterbi Decoder

The input given to the convolutional encoder is 10111000. After 8 clock cycles the encoded value is obtained as 1110000110011100. The output waveform of convolutional encoder is shown in figure 8.

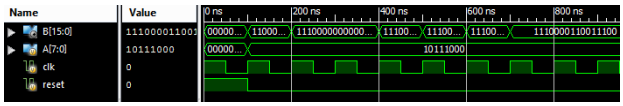

Fig.8 Output waveform of Convolutional encoder

The Viterbi decoder decodes 1110000110011100 and obtains the result after 8 clock cycles.

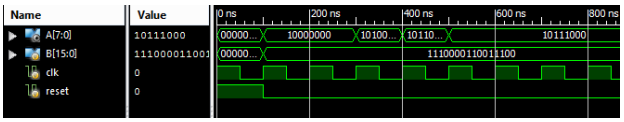

Fig.9 Output waveform of Viterbi decoder

D. Interleaver & Deinterleaver

The interleaver slices the input data to avoid burst errors. The output waveforms of both interleaver and deinterleaver are shown in figures 10 and 11 respectively.

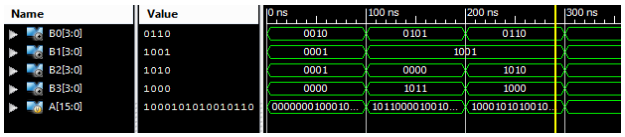

Fig.10 Output waveform of interleaver

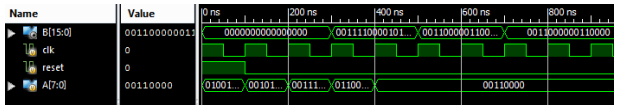

Fig.11 Output waveform of deinterleaver

E. QPSK Modulator & Demodulator

In QPSK modulation 2 bits of data are encoded at a time. Here the angles used are 0,90,180 and 270 degrees. The output waveform is shown in figure 12.

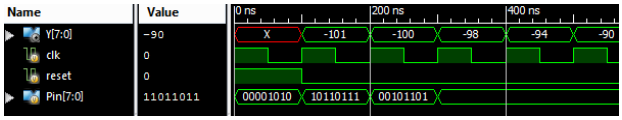

Fig.12 Output waveform of QPSK Modulator

The output waveform of a QPSK demodulator is shown below.

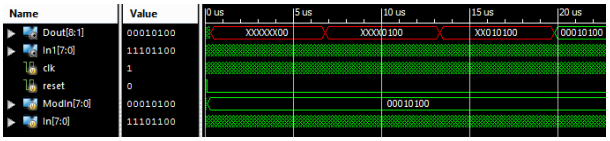

Fig.13 Output waveform of QPSK Demodulator

F. FFT & IFFT

The FFT and IFFT are used for conversion between time domain & frequency domain. The respective output waveforms are shown below.

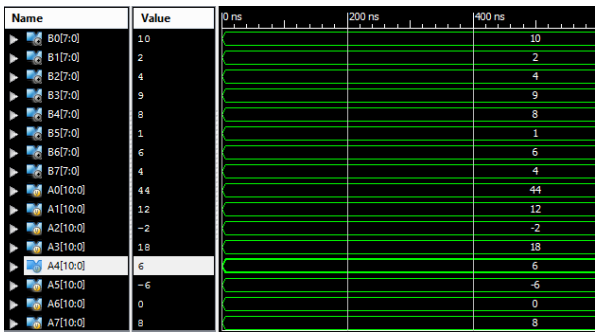

Fig.14 Output waveform of IFFT

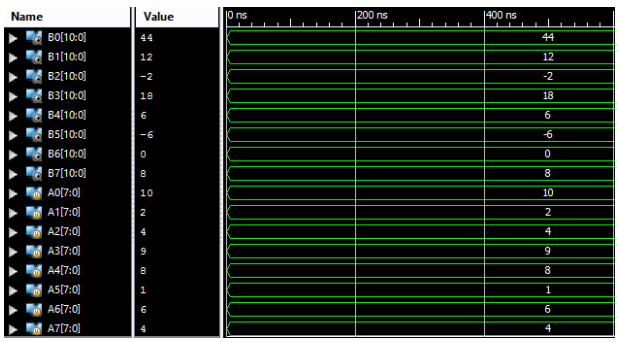

Fig.14 Output waveform of FFT

G. CRC

The figure 15 shows the output waveforms of the CRC. Since the received CRC and calculated CRC are different the retransmission request is made high.

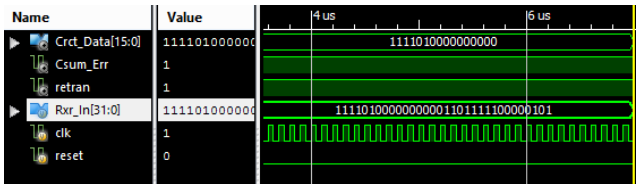

Fig.15 Output waveform of CRC

Figure 16 shows the design summary of the OFDM.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	23	4800	0%
Number of Slice LUTs	48	2400	2%
Number of fully used LUT-FF pairs	22	49	44%
Number of bonded IOBs	20	102	19%
Number of BUFG/BUFGCTRLs	1	16	6%

Fig.16 Device utilization summary.

Conclusions

An efficient OFDM transmitter and receiver have been implemented on Spartan 6 tyro kit designed by Pantech Solutions. The efficiency of the system is improved by improving the operation of the CRC. The CRC is improved in such a way that it can detect up to two bit errors and can correct single bit errors. Thus it saves a considerable amount of time when there occurs single bit errors. Verilog is used as the Hardware Description Language (HDL) to program all the components of the OFDM system and verification of functionality of all the components has done by giving different input and output using Xilinx ISE 14.2.

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