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Research Article

Performance Analysis of Multilevel Z-Source Inverter using Three Level NPC Inverter

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Abstract

The conventional Z-source inverter can be used for boosting the output voltage for the various applications of dc–ac, ac–ac, dc–dc, and ac–dc power conversion. The main limitation of Z-source inverter is voltage stress across the switches because of high boosting feature. This paper presents the performance analysis of Z-source multilevel inverter using three level NPC inverter to overcome the limitation of conventional Z-source inverter. Multilevel converters gives a flexibility to choose voltage levels as a supplementary control element and allows more alternatives to generate the output waveform. For this reason, the power quality of multilevel inverters have inherently upgraded, distinguished by: lower voltage distortion (more sinusoidal waveforms), diminished dv/dt, and lesser common-mode voltages, that will decrease or even remove the necessity of output filters. The topology is implemented in MATLAB Simulink environment in order to evaluate the performance, the model is tested with different modulation indices. The simple boost pulse width modulation scheme is used along with In-phase level shift modulation in the present work.

Keywords: *Z-source inverter; diode clamped multilevel inverter; shoot through duty ratio; modulation index; voltage stress; level shift modulation; neutral point clamped inverter*

1. Introduction

The conventional voltage and current inverters have been awfully bounded because their obtainable output voltage range is limited, short-circuit occurs due to misgating and some other theoretical difficulties also occurs owing to their bridge type structures. The z-source inverter topology was proposed in 2002 to conquer the traditional inverters (F.Z. Peng, 2003) problems, in which the traditional dc-dc boost converter function has been favorably recommended into the inverter by an unequalled X-shape impedance network. As far as research concern in power electronics, the Z-source inverter topology has been considerably analyzed from different prospect (F.Z. Peng, 2004; Jih-Sheng Lai *et al*, 1996), however in the open literatures the work related to its boost inversion ability and impedance network are barely reported.

The traditional Z-source inverter resides of an impedance network, having two capacitors and two inductors. In three phase Z-source inverter, there are nine switching states where as in the traditional voltage source inverter, there are eight switching states. So, the one extra state of the Z-source inverter is a shoot through state that determines the buck-boost feature to the inverter (M. Shen *et al*, 2004; Poh Chiang Loh *et al*, 2007).

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This way the Z-source inverter is different from voltage and current sources inverters (Jih-Sheng Lai *et al*, 1996). In low voltage energy sources such as fuel cell, photovoltaic etc, a recent technology is used in dc-dc power converts for growing power levels. It includes Switched-Capacitor (SC), Switched-Inductor (SL) and or combination of both (SC/SL). For this we can also consider the additive voltage cells, techniques without transformer and cascaded topologies. The most significant feature of these structures is acquiring great efficiency, large power density and simplest structures (F.Z. Peng *et al*, 2005). As the Multilevel converters gives a flexibility to choose voltage levels as a supplementary control element and allows more alternatives to generate the output waveform with lower voltage stress on switches (Jih-Sheng Lai *et al*, 1996; Xiangyang Xing *et al*, 2014). This paper combines the features of Z-source inverter and multilevel inverter in order to overcome the limitation of voltage stress problem of conventional Z-source inverter. The Z-source multilevel inverter topology is implemented based on three level diode clamped multi-level inverter. The topology is tested with simple boost pulse width modulation control with different modulation indices in the MATLAB Simulink.

2. Conventional Z-source Inverter

The Fig. 1, shows the impedance network of the Z-source inverter includes two split inductors (L_1 and L_2)

and two capacitors (C_1 and C_2) which are coupled in X-shape. The additional zero state can be made possible while the switching actions of upper and lower arms made possible, which determines the boost factor *B* for the voltage across the dc-link bus is expressed by:

$$B = \frac{V_{dc}}{V_{in}} = \frac{1}{1-2\frac{T_0}{T}} = \frac{1}{1-2D} \quad (1)$$

Where, T_0 is the shoot-through interval during a switching cycle *T* and *D* is the duty ratio of each cycle, which is equal to T_0/T.

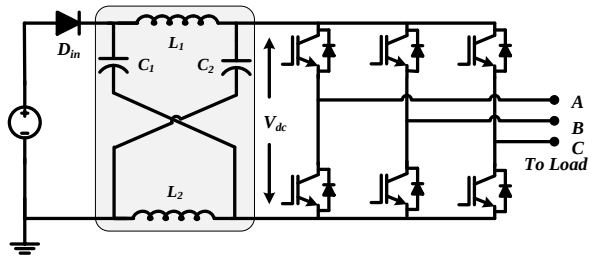

Fig.1 Conventional Z-source inverter.

From (1), it is observed that *D* is limited for the minimum scale of zero to the maximum of 0.5, in which the impendence network can execute the step-up dc-dc conversion from the input voltage V_{in} to the dc-link voltage V_{dc}.

Practically, a higher value of *D* is required to contribute a very high boost factor for the low voltage dc energy source. Thus, the Z-source inverter would have to be performed under the severe state of the shoot-through zero state. Accordingly, the modulation index, M of the main circuit will be reduced to a very low level, and the relations can be demonstrated by (1).

$$M \leq 1-D \quad (2)$$

Where,

$$M = \frac{\text{Amplitude of the modulation waveform}}{\text{Amplitude of the carrier waveform}} \quad (3)$$

The resulting lower modulation index values gives an inadequate boost inversion ability with high THD values. As a consequence, the quality of the performance of ac output will be reduced notably. For an optimal system design, the effective values of *D* have an upper limit, so the effective boost factor of Z-source impedance network is sincerely bounded according to (1).

3. Z-source NPC Inverter

The concept of Multilevel inverters are power-inversion systems possessed by an array of power semiconductors and capacitive voltage sources so, when accordingly connected and controlled, can produce a multiple-step voltage waveform with variable and controllable frequency, phase, and amplitude. The stepped waveform is symphonized by electing distinct voltage levels produced by the appropriate connection of the load to the different capacitive voltage sources. The above connection is achieved by the appropriate switching of the power semiconductors as shown in Fig. 2 (P. Chiang Loh *et al*, 2007).

The number of levels of an inverter can be specified as the number of steps or constant voltage values which can be produce by the inverter between the output terminal and any arbitrary internal reference node within the inverter. Usually, it is a dc-link node, and it is commonly denoted by N and called neutral. To be termed as a multilevel converter, each phase of the converter needs to produce minimum of three different voltage levels which discriminates the conventional two-level voltage source converter (2L-VSC) from the multilevel family.

Two-level converters can develop a variable frequency and amplitude voltage waveform by adjusting a time average of their two voltage levels. This is commonly accomplished with pulse-width modulation (PWM) techniques. Multilevel converters gives a flexibility to choose voltage levels as a supplementary control element and allows more alternatives to achieve the output waveform. For this reason, the power quality of multilevel inverters have inherently upgraded, distinguished by: lower voltage distortion, diminished *dv/dt*, and lesser common-mode voltages, that will decrease or even remove the necessity of output filters (A. Nabae *et al*, 1981; P. Chiang Loh *et al*, 2007; Xiangyang Xing *et al*, 2014).

Consider, a three-phase system, the levels of one phase are integrated with those of the other phases, producing more different levels in the line-to-line voltage. For a converter with 'n' phase to neutral voltage levels, (2n−1) levels can be found in the line-to-line voltage. The same thing appears in the three-phase load voltage, in which sequence of the line voltages are generated, and acquiring (2n−1) voltage levels. Though, number of levels of inverter is represented by 'n' only.

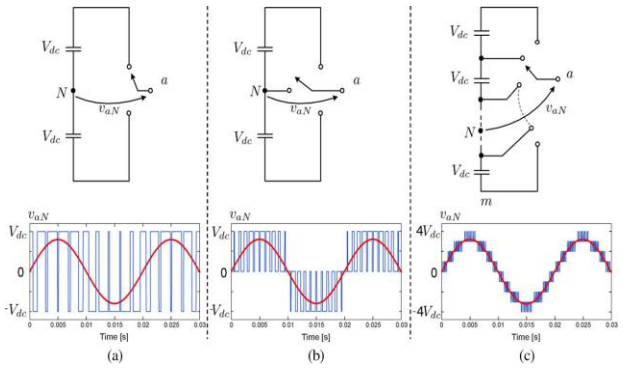

Fig.2 Output voltage waveform: of inverter a) two level, b) three level, c) nine level

As the conventional Z-source inverter operates in two different modes of shoot through and non-shoot through states, the three level Z-source inverter can also operate in the same modes but the shoot through state will be divided into three sub categories namely full shoot through, upper shoot through and lower shoot through states (P. Chiang Loh *et al*, 2007).

In this paper, the performance of Z-source neutral point clamped three level inverter is evaluated.

3. Concept of Z-source to NPC Inverter

The shoot through states in Z-source multilevel inverter are further divided into full shoot through (FST), upper shoot through (UST) and lower shoot through (LST). These shoot through switching states are explained by considering one phase leg of multilevel inverter shown in Fig. 3. There are three kinds of switching state which generates three kinds of levels as P, N, and O.

- Positive Level 'P': S_{a1}, S_{a2} are on, S_{a3}, S_{a4} are off.
- Negative Level 'N': S_{a1}, S_{a2} are off, S_{a3}, S_{a4} are on.
- Zero Level 'O': S_{a1}, S_{a4} are off, S_{a3}, S_{a2} are on.

Though, Z-source NPC inverter has three additional switching states in each phase leg as described in Table. 1. These additional switching states are full shoot-through (FST), upper shoot-through (UST) and lower shoot-through (LST). In Table 1, switch ON and OFF positions are indicated with logic 1 and 0 respectively (C.L. Kuppuswamy, 2013).

These shoot-through state is allowable in Z-source NPC inverter because it gives the boosts the dc link voltage to the inverter.

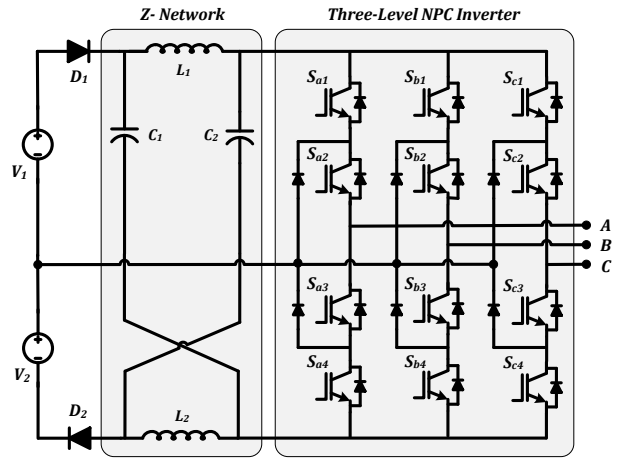

Fig.3 Z-source three level NPC inverter

A. Operating principle

1) Non-shoot-through state

The non-shoot-through state coincides to the six active states and two zero states of the main circuit, and the equivalent circuit is shown in Fig. 4(a). In each switching cycle, the two non-shoot-through zero states are used along with two adjacent active states to integrate the required voltage. In non-shoot-through state dc voltage is high enough to produce ac output voltage. Now to complement the depleted energy of C_1 and C_2 during the shoot-through state, C_2 is charged by V_1 and and C_1 is charged by V_2.

Table 1 Switching states of Phase leg 'A'

State	Switching combination				Diode combination				Output voltage
	Sa_1	Sa_2	Sa_3	Sa_4	D_1	D_2	Da_1	Da_2	
NST	1	1	0	0	ON	ON	OFF	OFF	$V_i/2$
NST	0	1	1	0	ON	ON	ON	ON	0
NST	0	0	1	1	ON	ON	OFF	OFF	$-V_i/2$
FST	1	1	1	1	–	–	–	–	0
UST	1	1	1	0	ON	OFF	OFF	ON	0
LST	0	1	1	1	OFF	ON	OFF	ON	0

2) Shoot-through state

The shoot through state is further divided into full shoot-through (FST), upper shoot-through (UST) and lower shoot-through (LST). Here we will consider the one phase leg to explain the shoot through state of multilevel inverter. In Full shoot through state all the switches S_{a1}, S_{a2}, S_{a3} and S_{a4} of phase leg A will be in on state. Z-network is disassociated from the input dc source when the diodes D_1 and D_2 will become reverse biased.

Fig. 4(b) shows the upper shoot-through which is created by switching "on" of switches S_{a1}, S_{a2} and S_{a3} of the phase leg A. The UST operating state results into blocking of diode D_2.

In the same manner, Fig. 4(c) shows the lower shoot-through state which is generated by switching "on" of S_{a2}, S_{a3} and S_{a4} of the phase leg A . The LST operating state results into blocking of diode D_1.

4. Derivation of boost factor of Z-source NPC

For the convenience, it is considered as inductors and capacitors have the same inductance (L) and capacitance (C), respectively. Let the input DC voltage (V_i) is the sum of two separate dc sources V_1 and V_2. The Z-network is connected in between the two separated dc sources at input side and the three level NPC inverter at output side. For the simplicity of derivation assume V_1 and V_2 are having the same magnitude of E. So voltage expression for NST state is expressed as

$$V_L = 2E - V_C \tag{4}$$

$$V_P = +\frac{V_i}{2}, V_N = -\frac{V_i}{2} \tag{5}$$

$$V_i = 2(V_C - E) \tag{6}$$

Voltage expression for UST and LST state are as follows:

UST

$$V_{L1} = E \tag{7}$$

$$V_P = 0, V_N = E - V_{C1} \tag{8}$$

LST

$$V_{L2} = E \tag{9}$$

$$V_P = -E + V_{C2}, V_N = 0 \tag{10}$$

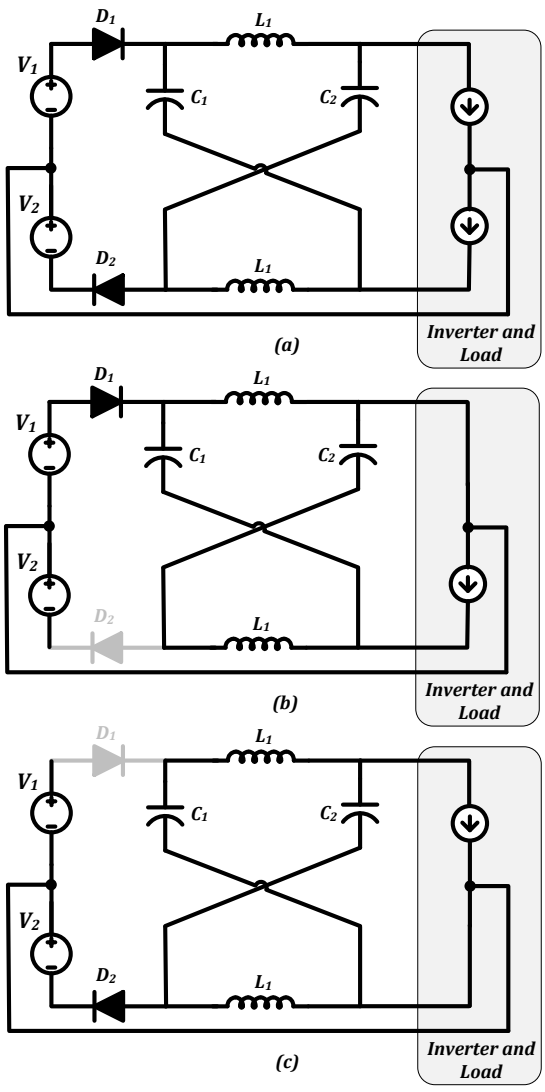

Fig.4 Equivalent circuits (a) Non-Shoot through state; (b) Upper shoot-through state; (c) Lower shoot-through state

The duration of the NST, UST and LST states is denoted by T_N, T_U, T_L, respectively. Consider T_U and T_L are equal and the total upper shoot-through and lower shoot-through duration by T_0. During steady state, the average voltage across the inductors is zero. So, expressions are as follows

$$\frac{(2E - VC)T_N + ET_U}{T} \tag{11}$$

$$T_N + T_U + T_L = T \tag{12}$$

From (11) and (12) V_C can be expressed as

$$V_C = \frac{2E(1 - T_0/2T)}{1 - T_0/T} \tag{13}$$

The dc-link voltage can be obtained by substituting (13) into (6) during NST state as

$$V_{i\_NST} = \frac{2E}{1 - T_0/T} \tag{14}$$

We have dc link voltages while substituting (13) into (8) and (10) during UST and LST state as

$$V_{i\_UST} = V_{i\_LST} = \frac{E}{1 - T_0/T} \tag{15}$$

Now compare equation (14) and (15) we can see that the dc link voltage is higher in the NST states which is twice the dc link voltage present when it is in UST and LST states.

The fundamental peak ac output voltage V_{Xo} is expressed by (16) and (17).

$$V_{XO} = \frac{M}{\sqrt{3}} V_{i\_NST} \tag{16}$$

$$V_{XO} = \frac{1}{1 - T_0/T}\{\frac{M}{\sqrt{3}}(2E)\} = B\{\frac{M}{\sqrt{3}}(2E)\} \tag{17}$$

Where B is the boost factor, which is always ≥ 1.

5. Modulation scheme of Z-source NPC

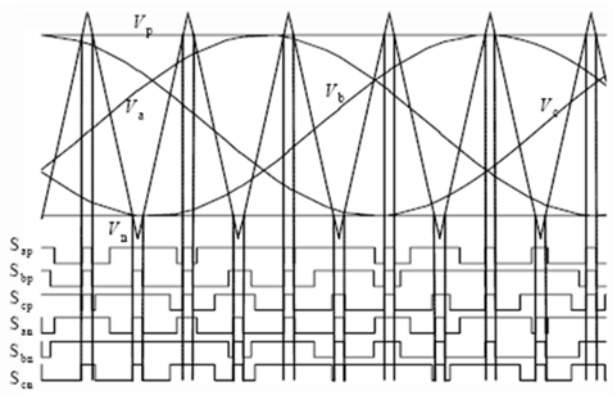

Fig.5 Simple boost PWM

The above figure describes the simple control method which uses a straight line equal to or more than the peak value of the three phase attributes to control the shoot-through duty ratio in a traditional sinusoidal PWM. The Z-source multilevel inverter sustains the six active states unaltered as the traditional carrier based

PWM control, for this simple boost control (C.L. Kuppuswamy, 2013), the resultant shoot through duty ratio diminished with the increase of the modulation index, M. The limitation of maximum shoot-through duty ration of simple boost control is (1-M), so it reaches zero at a modulation index of one. So to obtain an output voltage having high voltage gain, a small modulation index value has to be used.

6. Simulation Results

In order to evaluate the performance of Z-source NPC inverter, the model is implemented in the MATLAB Simulink by considering the input DC voltage (V_i) of 150 V, Z-network consists of $L_1 = L_2 = 5$ mH and $C_1 = C_2 = 1000$ µF. The three phase resistive load of 5 kW is selected

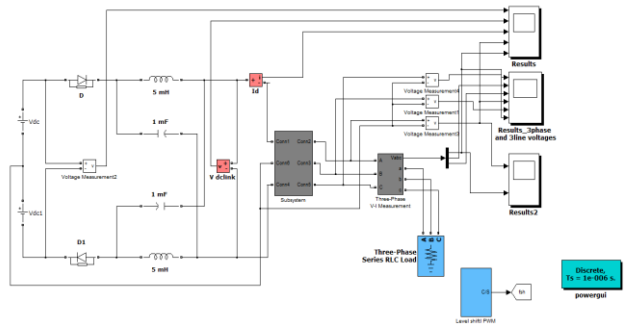

Fig.6 Simulink model of Z-source NPC inverter

Fig.6 shows the Simulink model implemented for the Z-source three-level inverter in the MATLAB Simulink. It has been examined for the three phase resistive load of 5 kW by using simple boost pulse width modulation. The switching frequency is chosen as 1 kHz.

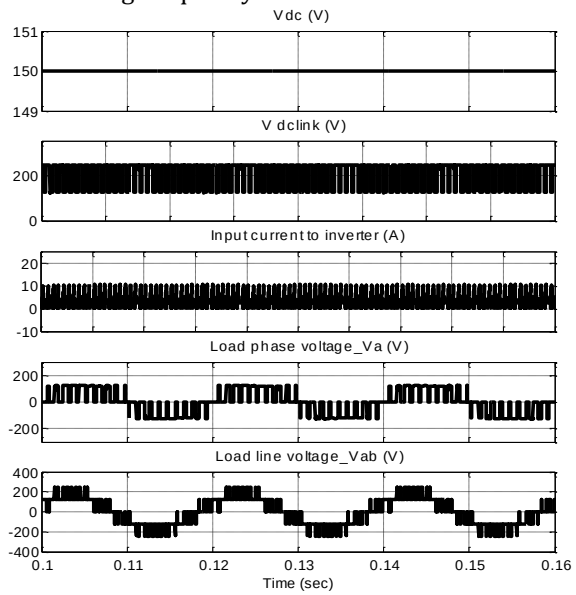

Fig.7 Simulation results of Z-source NPC showing (a) input DC voltage, (b) DC link voltage after Z-network, (c) Input current to the inverter, (d) Load phase voltage, (e) Load line voltage

The simulated scope results for the modulation index of 0.8 are shown in Fig. 7. From the results it has been clear that the output phase voltage is greater than the input DC voltage. That means output voltage is boosted to the higher level as 122 V of peak magnitude, whereas input DC magnitude is of 150 V. From (16), the voltage gain can be calculated as 3.93 for the above simulation. Fig. 8, shows the all the three phase load line and phase voltages.

A. Performance of Z-source NPC inverter for different modulation index values

The model is examined for the different modulation index values in order to evaluate the performance. The modulation index is varied from 0.6 to 0.9 and the captured results are shown in Fig. 9-12.

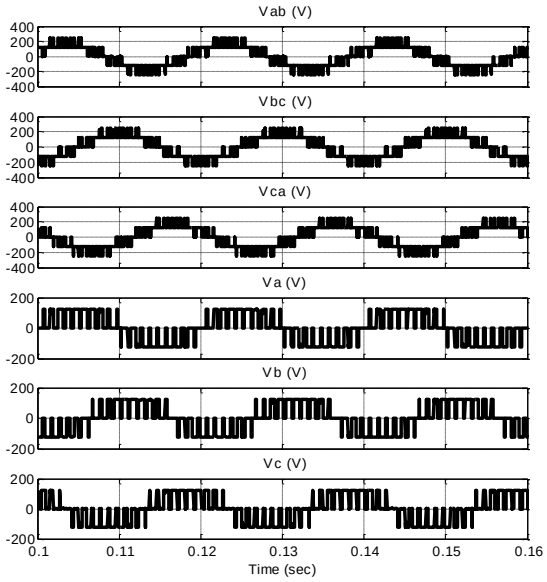

Fig.8 Scope results of Z-source NPC showing three phase load line and phase voltages

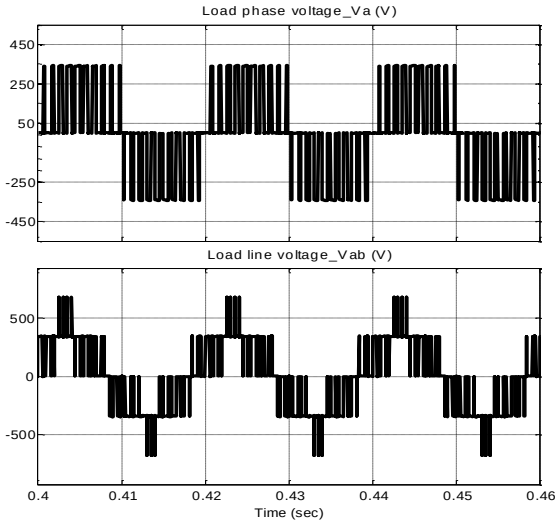

Fig.9 Phase and line voltage waveforms with modulation index of 0.6

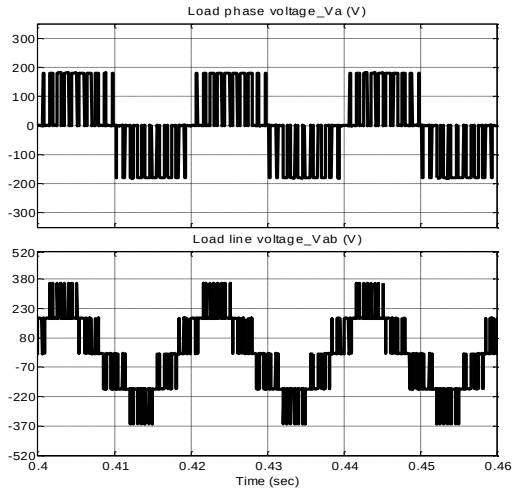

Fig.10 Phase and line voltage waveforms with modulation index of 0.7

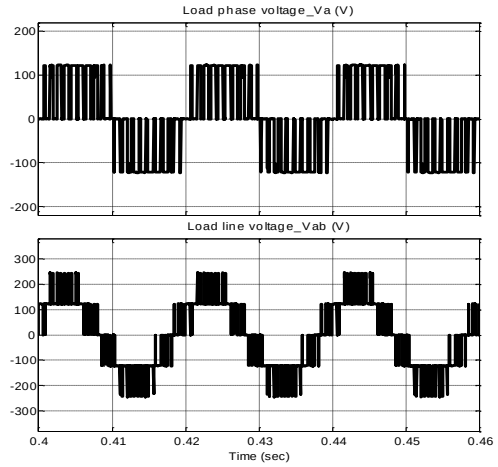

Fig.11 Phase and line voltage waveforms with modulation index of 0.8

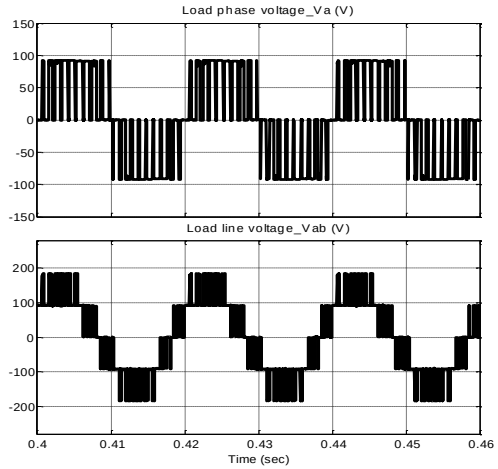

Fig.12 Phase and line voltage waveforms with modulation index of 0.9

As modulation index is increased the output load voltage is decreased because of the decreased shoot through interval same as that of conventional Z-source inverter. The results are summarized in the following Table 1.

Table 2 Peak value of load phase and line voltages with different modulation index values

Modulation Index (m)	Fundamental load voltage		Peak load voltage	
	Phase (V)	*Line (V)*	*Phase (V)*	*Line (V)*
0.6	205.9	326.7	344	681
0.7	126.5	219.0	181	360
0.8	97.6	169.0	122	244
0.9	82.6	143.1	92	184

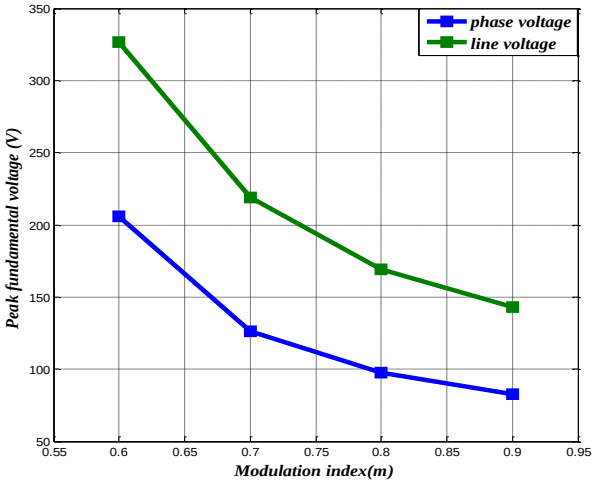

Fig.13 Change of peak fundamental value of load phase and line voltage with respect to modulation index

Conclusions

The Z-source multi-level inverter achieves voltage buck-boost in single stage without an addition of extra power electronic switches. The model is implemented in MATLAB Simulink. The model is investigated for the different modulation index values in order to estimate the performance. The performance analysis of the model is carried out with different modulation indices. As modulation index is increased the output load voltage is decreased because of the decreased shoot through interval. The control strategy is implemented for the suggested topology using simple boost control.

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