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Research Article

A 7-Input Minority gate design using Carbon Nano Tube Field Effect Transistor (CNTFET)

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Abstract

Carbon Nano Tube Field Effect Transistors (CNTFET) Technology are being widely studied as the alternative to the conventional Complementary Metal Oxide Semiconductors (CMOS) Technology. .Due to the increased demand of high speed processors, compact circuits, smaller dimensions and lower power consumption of integrated circuits has made Engineers and designers a challenging issues of technology scaling of electronic devices. Hence it is now necessary to adopt and study new materials and technologies. In this project, we proposed a design of CNTFET–based digital circuit and compared it with the existing CMOS technology based logic gates . For CNTFET-based circuits, the compact SPICE model can be used for simulations, which is the standard model that has been designed for simulating one or more CNTs devices by Standford University. The performance of CNTs can be evaluated in terms of power, delay, and PDP at room temperature. In this project a novel 7-input minority gate is proposed in CNTFET technology with 9 CNTs . With this proposed implementation of 7-input minority gate, different logic gates such as a 4-input NOR and 4-input NAND gates can be design which gives better performance in terms of its delay and energy efficiency with more driving power outputs.

Keywords: *Nano Electronics, Carbon Nano Tube, HSPICE, Digital Logic Gates, Carbon Nano Tube Field Effect Transistors.*

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1. Introduction

As predicted by Gordon Moore in 1965, that the number of transistors in chips duplicates every 18 months which faces new challenges and limitations (Moore *et al* 1998) . Hence Complementary metal oxide semiconductor (CMOS) is no more suitable for near future nano-scale regime due to its limitations as Lithography, huge parametric variations, and high power density (Boykin *et al* 2011). To overcome these difficulties and challenges in sub-nano meter scale new technologies have emerged. Along with these novel technologies such as, carbon nano tube field effect transistor (CNTFET), quantum-dot cellular automata (QCA) Benzene ring transistors and single electron transistor (SET), CNTFET looks to be more feasible because of its CMOS-like structure (Kim *et al* 2010) . Carbon nano tubes have excellent electrical performance such as higher sub-threshold slope, lower short-channel effect, lower leakage current (compared with Si-MOSFET) (Fregonese *et al* 2008) . Hence it makes CNTFET more promising in performance and is being used by designers for designing simple digital circuits such as SRAM, ring oscillators, Logic gates, Majority and Minority circuits etc.

2. Carbon Nano Tube

The first person to see carbon nano tubes was Sumio Iijima of NEC Crop in Tokyo, who discovered them in 1991 while studying electron microscope images of the soot produced by electrical discharges between carbon electrodes (Sinha *et al* 2013). A CNT is a hollow cylinder constructed by rolling up a sheet of graphene. Graphene is a single atomic layer of graphite which in turn is a crystalline form of carbon. Carbon nano tubes are cylinders with diameters ranging from 1 nm to 50 nm and length, over 10µm. The carbon atoms are arranged into hexagons that form a honeycomb pattern (Boykin *et al* 2011).

A nano tube with multi layer or single layer viewed is a graphite sheet rolled into a cylinder as shown in Fig. 1. Hence there are two types of nano tubes as single-wall nano tube (SWCNT) which is made up of single graphite sheet and a multiwall nanotube (MWCNT) consists of multiple graphite shells. The graphene is rolled and is described by a pair of indices (n, m), in such a way that known as chiral vectors, and these vectors determines its metallic or semiconducting type of CNT (Fregonese *et al* 2008) . Most single-walled nano tubes (SWNT) have

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approximate diameter of 1 nanometer, with a longer tube length which can be many millions of times long (Tapiwala *et al* 2014) (Fregonese *et al* 2008) .The structure of a SWNT can be examined by casing a one-atom-thick layer of graphite sheet called graphene into a faultless cylinder (Boykin *et al* 2011). The way graphene is rolled and is described by a pair of indices (n, m) where integer's n and m denote the number of unit vectors along two directions in the honeycomb crystal lattice of graphene. If m = 0, the nano tubes are zigzag nano tubes, and if n= m, the nano tubes are armchair nano tubes (Fregonese *et al* 2008) (Boykin *et al* 2011). Otherwise, they are known as chiral.

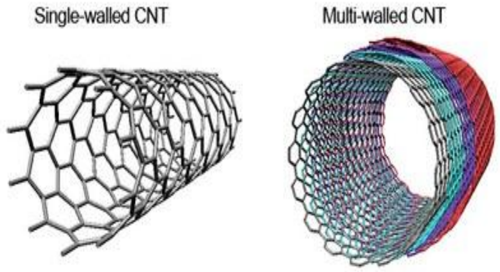

Fig.1 Structure models of nanotube

Hence the diameter of an ideal nanotube can be calculated from its indices (n, m) is as follows

$$d = \frac{a}{\Pi}\sqrt{(n2+nm+m2)} = 78.3\sqrt{((n+m)2-nm)}\,pm \qquad (1)$$

Where a =0.246 nm

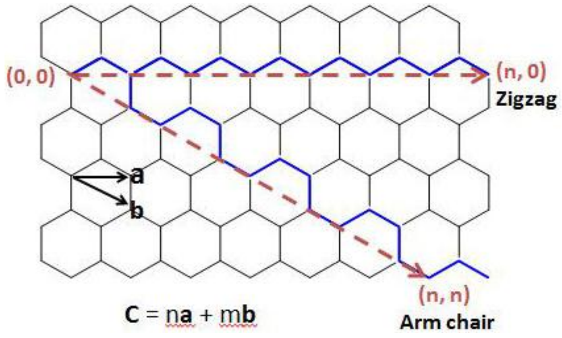

Fig.2 Graphene sheet representation by (n, m)

The indices (n,m) nano tube with (**C**) as its vector is an infinite graphene sheet which describes how to roll up to make it nano tube. Here in this sheet we use T to denotes the tube axis and a, b are the unit vectors of the sheet in real space as shown in Fig.2 (Fregonese *et al* 2008).

CNTs' electrical conductivity can be varied by doping them with impurity atoms. In this way both p-type and n-type CNTs can be obtained which then enables the creation of complementary logic structures such as those adopted in conventional CMOS design. (Boykin *et al* 2011). In graphite (and hence in CNTs) the atoms of carbon are very closely packed in the basal planes, the distance between their centers (nearest neighbor distance) being only 1.42 (Sinha *et al* 2013). Å, which is even closer than in diamond. One consequence of this small nearest-neighbor distance is that impurity species are unlikely to enter the covalently bonded in-plane lattice sites substitutionally but rather occupy some interstitial position between the graphene layer planes which are bonded by a weak van der Waals force. The only impurity atom that can easily do this is boron, hence, CNTs are usually doped using boron atoms; however, alkali metals and halogens such as bromine and iodine are also used. CNTs can exhibit either semiconducting or metallic behavior depending on their chiral angle. The conductivity and robustness of metallic nano-tubes make them suitable for future interconnects. As for the semiconducting CNTs, they exhibit the desired properties for making field effect transistors. The restricting issue here is to selectively separate metallic and semiconducting CNTs.

3. Carbon Nano Tube Field Effect Transistor (CNTFET)

A single carbon nano tube is positioned as a bridge between two electrodes. Here the electrodes act as the source and drain of the transistor, while nano tube plays a role of the channel, as shown in the schematic Fig. 3. However, in fig.4 the CNFET circuits in planar and co-axial form which has been simulated with the help of nanohub website is shown. The nano tube is on or off as we apply the appropriate voltage to gate. The first carbon nano tube field-effect transistors (CNTFETs) was introduced in 1998 (Fregonese *et al* 2008) . Then CNTFET is a multi gate functioning device. In this device, the transistor action occurs at the contact points between the metal electrodes and carbon nano tube. Hence the CNTFETs have been manufactured with the help of semiconductors, as they show promising results due to their superior electrical characteristics over silicon based MOSFETs .

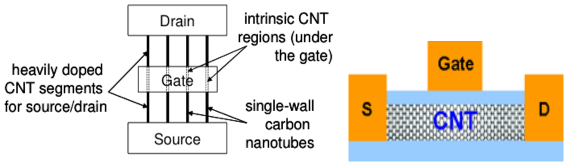

Fig.3 Schematic of CNTFET

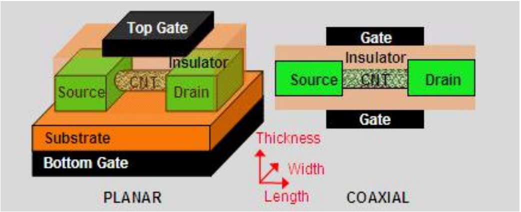

Fig.4 CNFET circuit in Planar and Coaxial Types [www.nanohub.org]

In terms of the device working procedure, CNFET can be defined by two categorized as either Schottky Barrier (SB) controlled FET or MOSFET-like FET. The ambipolar behavior of SB-controlled CNFET makes it undesirable for complementary logic design. Considering both the fabrication feasibility and superior device performance of the MOSFET-like CNFET as compared to the SB-controlled FET (Boykin *et al* 2011). An Ideal MOSFET-like CNFET is formed by 1 or more semiconducting CNTs perfectly aligned and well-positioned whose section under the gate is intrinsic and the s/d extension regions are n/p doped (Tapiwala *et al* 2014).

4. Comparison to MOSFETS

CNTFETs show different characteristics compared to MOSFET in their performances. The p-CNTFET produces ~1500 A/m of the on-current per unit width at a gate overdrive of 0.6 V while p-MOSFET produces ~500 A/m at the same gate voltage ,in a planar gate structure (Sinha *et al* 2013). Hence the on-current advantage which comes from the high gate capacitance helps to improve the channel transport factor. Since the effective gate capacitance per unit width of CNTFET is double that of a p-MOSFET, thus the compatibility with high- k gate dielectrics becomes a definite advantage for CNTFETs (Boykin *et al* 2011) . About twice the higher carrier velocity of CNTFETs comes from the increased mobility and the band structure than usual MOSFETs. CNTFETs, in addition, have about four times higher trans-conductance as compared to MOSFETs.

5. Proposed Work

Minority function which has complementary behavior of majority function, is a complete function gate because it has capability of implementing other gates such as NAND and NOR. A 7-input minority gate has 7 binary inputs and its single output will be equal to '1' when 3, 2, 1 or none of the inputs are '0' and if not the output will be '0' (Moaiyeri *et al* 2013) . Minority vote of inputs can be considered as complementary of carry-out of arithmetic summation. Minority function is used for data mining and it is also used in the voting systems. Design of a 7-input minority function seems to be important because in some cases fast and minimum cost logical gates with large fan-in are required. Designing such a 7-input minority function gate which derives 4-input logical gates such as NAND, NOR, AND and OR (Tapiwala *et al* 2014).

Becomes easier and more reliable since majority-based structures are utilized not only in conventional fault-tolerant architectures but also in new nano-scale technologies. Implementing such 7-input minority function in conventional method by using sum of products (SOP) is difficult and costly, especially when it is implemented in conventional CMOS style that the number of transistors multiplied with two due to the pull- down and pull-up networks.

The proposed 7-input minority function gate, shown in Fig. 5, has seven CNTFETs that each of them acts as a capacitor and are connected to a CNTFET-based inverter (Moaiyeri *et al* 2013) . The truth table of 7-input minority function has 2^7 =128 rows. For reducing the size of the truth table, the summation of inputs, as Shown in given below Table 1, is referred.

Now we describe the structure of our proposed block diagram. The middle point of the circuit, shown by 'M' in Fig. 4, has a voltage corresponding to the scaled sum of inputs (Moaiyeri *et al* 2013). As a result the voltage level at this point can be expressed by the below given equation

$$Vm = \frac{1}{\#inputs}\sum_{i=1}^{7} Xi \tag{2}$$

Table 1 Truth Table of 7-input minority function

∑inputs	7minority
0	1
1	1
2	1
3	1
4	0
5	0
6	0
7	0

A minority function is genetically a voter, but instead of absorption of the majority vote, it shows the minor vote at its output, (Moaiyeri *et al* 2013) and due to the specified threshold of an inverter which is utilized to generate the expected output as given in below relation.

$$InverterThreshold \propto \lfloor \#inputs/2 \rfloor \tag{3}$$

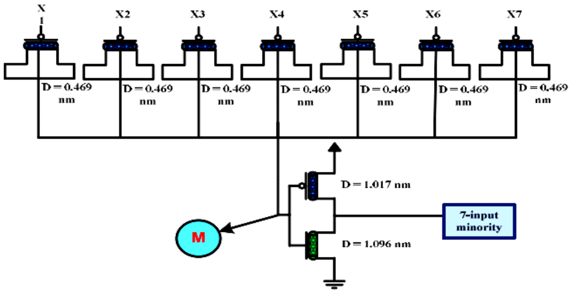

Fig.5 Proposed design of 7-input minority function

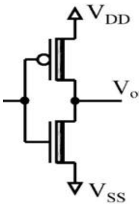

Fig.6 Proposed design of Inverter

The CNTFET inverter circuit is shown in Fig. 6. It consist of a p-type and n-type Cnt . Here the simulation is performed on HSPICE with the help of Standard CNFET model.

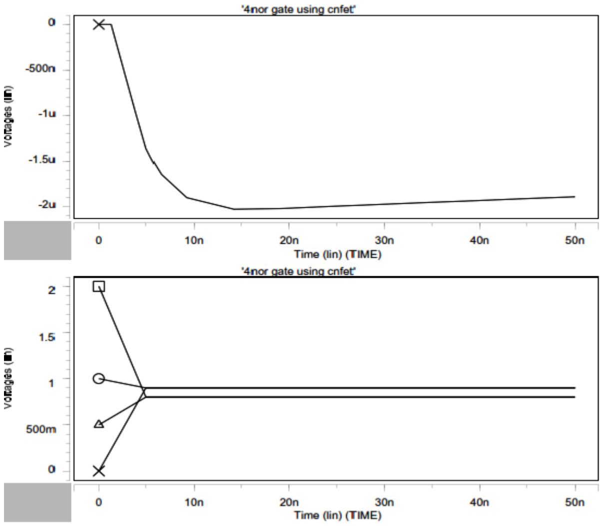

Fig 7.4-input NOR Gate input/output wavefrom

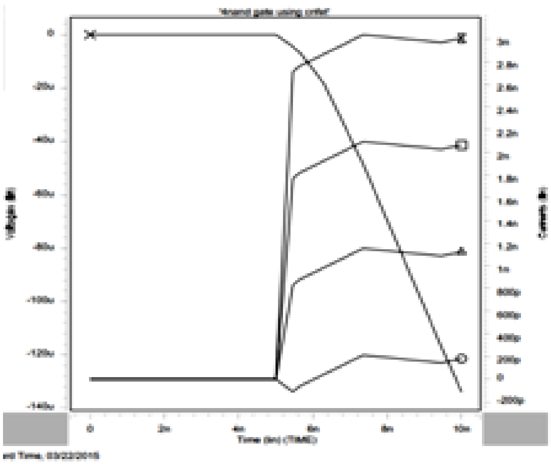

Fig 8.4-input NAND Gate input/output wavefrom

Conclusions

In this work a CNFET-based 7-input minority function logic gate is proposed which can be also used for designing different 4-input logic gates (Moaiyeri *et al* 2013) . The CNFET-based logic gates are simulated in 32-nm technology in HSPICE software using Stanford University's CNFET HSPICE Model and BSIM PTM Model respectively. Here Fig.7 and Fig.8 shows the simulated input and output waveforms of 4-input NAND & NOR gate using CNTFET based minority function.

The simulations are carried out at room temperature for different values of supply voltages i.e. 0.9V, 0.8V and 0.7V, and performances are studied in terms of power, delay and PDP is shown in table 2. The CNFET-based logic gates show far better results as compared to those of CMOS-based logic gates.

Table 2 Simulation result of proposed minority gate vs power supply

VDD(V)	Delay (p sec)	Power (micro W)	Energy Consumption (J)
0.7	72.3	0.45	3.98
0.8	58.3	0.792	4.61
0.9	23	2.25	5.18

This work concerned a study of the performance of CNT-based electronic circuits in the presence of process parameter variations. CNT diameter variations are one of the main sources of variation which can cause CNFET drain current variations and hence irregular time and energy consumption behavior.

The effects of diameter variations on basic logic structures (NOT, NAND and NOR) were examined using . It was found that variation in propagation delay decreases as the diameter of CNTs was increased.
Energy usage of the logic gates was measured using the Power Delay Product (PDP). This work further shows that greater energy efficiency is obtained for logic gates utilizing wider CNT diameters

Future work

The most desirable future work involved in CNTFETs will be the transistor with higher reliability, lower production cost, or more enhanced performances. For example, such efforts could be made by adding effects external to the inner CNT transistor like the Schottky barrier between the CNT and metal contacts, multiple CNTs at a single gate, channel fringe capacitances, parasitic source/drain resistance, and series resistance due to the scattering effects.

This work can be improved further by a thorough examination of more complex logic functions and memory structures. This work has only considered 4-input logic structures. A study with such higher input structures (i.e. 4 input logic gates) would be useful, as stacking and the ensuing body effect will become involved (Moaiyeri *et al* 2013) . As the body effect is concerned with changes in the threshold voltage and Vth in CNTs is directly related to CNT diameter this would be a particularly interesting study to carry out.
Ensuring that CNTs are positioned in a straight line under the gate between the source and drain is a very difficult task. In most cases multiple CNTs are present under each CNFET gate and in all likelihood they are not completely in parallel with each other. This could then prevent the CNTs under the same gate from being in common-mode and experience varying voltage changes along their lengths hence changes in capacitance can occur. Being able to address this problem would be a major breakthrough in the area of CNFET design (Sinha *et al* 2013).

Also as CNTs in practice are often not aligned in a straight line and not parallel to each other, the length of the CNT under the gate can vary. This means that a constant channel length cannot be assumed and channel length variations become an issue. A study of CNFET logic performance in the presence of various sources of variations at different technology nodes could be the next step towards future work.

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