International Journal of Current Engineering and Technology
E-ISSN 2277 – 4106, P-ISSN 2347 – 5161

Available at http://inpressco.com/category/ijcet

General Article

Multilevel Inverters – A Survey

Vijay Y. Patil†* and V.V.Patil†

†JJMCOE, Jaysingpur, Maharashtra, India

Accepted 31 May 2015, Available online 01 June 2015, **Vol.5, No.3 (June 2015)**

Abstract

Multilevel inverter is an effective & practical solution for increasing power demand & reducing harmonics of AC waveforms. Multilevel inverter provides a desired output voltage from several levels of DC voltages as inputs to inverter. It has been found that this technique reduces the switching losses & total harmonic distortion. Advantage of the multilevel inverters is that they can generate output voltages with very low distortion and dv/dt. Also generate smaller common-mode voltage and operate with lower switching frequency compared to the conventional two level inverters. With use of lower switching frequency result in low switching losses & also reduced and the dv/dt. The voltage steps are smaller, as the number of levels increase.

Keywords: *H-bridge Inverter, Multilevel Diode Clamped Inverter, Cascaded MLI, PWM Inverter*

Introduction

Multilevel inverter is a power electronic converter that generates desire output voltage with varying DC voltage as input. We can achieve output sinusoidal signal near to the fundamental waveform as we varying the input DC levels (Siriroj Sirisukprasert *et al*, 2002). The primary advantage of multilevel inverter is their small output voltages, results in higher output quality, lower harmonic component, better electromagnetic compatibility & lower switching losses. High magnitude sinusoidal voltage with extremely low distortion at fundamental frequency can be produced at output with the help of multilevel inverters by connecting sufficient number of DC levels at input (Lai.J.S *et al*, 1996). The cascaded H- bridge inverter & its derivatives are the most common topologies. Main advantage of this topology is that rating of the switching devices is highly reduced to rating of each cell. This number is quite high & may increase the circuit complexity, in turn reduce its reliability & efficiency. Cascaded H-bridge inverter has a modularized layout & the problem of the DC link voltage unbalancing does not occur, it is easily expanded to multilevel. However for this topology large number of switching devices are required which equals to 2(K-1) where K is number of levels.

Full-bridge or “H-bridge” Voltage Source Inverter

There are two control methods for this topology. The first one treats the switches (S_1, S_4) and (S_2, S_3) as a pair. This means that they are turned on and off at the same time and for the same duration. For square-wave operation the switches S_1 and S_4 are on for half of the period. For the other half, the pair of S_2, S_3 is turned on. Like the single-phase half-bridge VSC, the direction of the output current i_0 determines the conduction state of each semiconductor (Rodriguez, J *et al*, 2002).

When the two switches S_1 and S_4 are turned on, the voltage at the output is equal to the DC bus voltage V_{dc}. Similarly, when the switches S_2 and S_3 are turned on the output voltage is equal to - V_{dc}. Such circuit operation is illustrated in Figure below.

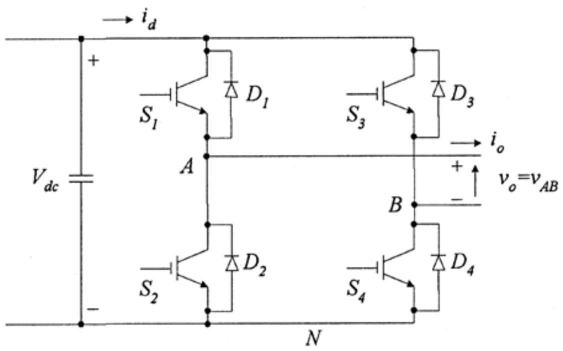

Fig.1 Full-bridge or “H-bridge” voltage source Inverter

In the first case, when the direction of the output current i_o is positive as shown in Figure 1,the current flows through switches S_1 and S_4 and the power is transferred from the DC side to the AC on ($t_4<t<t_5$). When the current becomes negative, although the switches S_1 and S_4 are turned on, the diodes D_1 and D_4 conduct the current and return power back to the DC

*Corresponding author: **Vijay Y. Patil**; **Dr. (Mrs.)V.V.Patil** is working as Professor

bus from the AC side $t_3<t<t_4$). For the other half of the period, when the switches S_2 and S_3 are turned on and the current is positive, the diodes D_2 and D_3 conduct ($t_1<t<t_2$). In this instance, power is transferred also back to the DC side from the AC side. Finally, when the current is negative, the switches S_2 and S_3 carry the current and assist the converter to transfer power from the DC bus to the AC side ($t_2<t<t_3$). In summary, there are four distinct modes of operation for this converter when the control method shown in Figure below is employed (two inverter modes and two rectifier modes). Simply said, at all times two switches are turned on and the legs are controlled in a synchronized way. The output voltage $v_0 = v_{AB}$ is shown in Figure 2 (a). The output current i_0 and the input DC current i_d are also plotted in Figures above (b) and (c) respectively. Similarly, like the case of the half-bridge topology, the square-wave generated across the AC side includes all odd harmonics and being a single-phase system, the third harmonic is also present (Figure above (d)). These harmonics when reflected back to the DC side source include all even harmonics figure above (f).

Demerits

High dV/dT ratings for switches (IGBT).
Higher harmonic distortions at O/P.
Higher Switching losses.

Multilevel Diode Clamped/Neutral Point Inverter, NPCMLI

In the NPCMLI topology the use of voltage clamping diodes is essential.

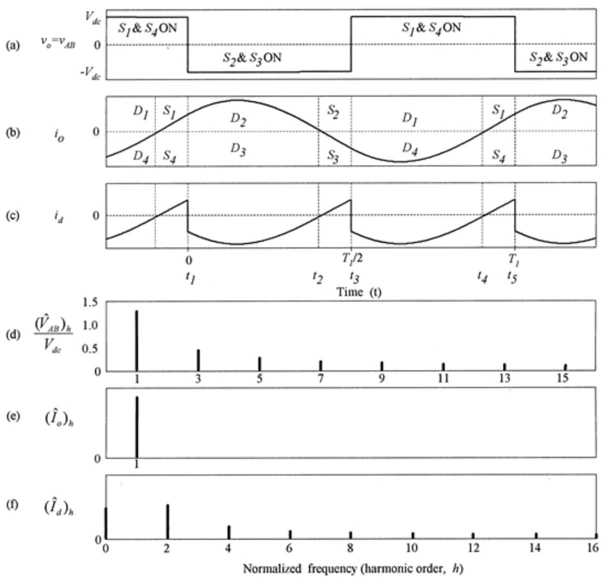

Fig. 2 Output waveforms of H-bridge Inverter

Figure 3, displays one phase-leg of a five-level NPC inverter. Input DC-bus is divided by an even number, depending on the number of voltage levels in the inverter. Also use of bulk capacitors in series with a neutral point in the middle of the line (left part of figure 3). Clamping diodes connected to an m-1 number of valve pairs, where m is the number of voltage levels in the inverter to the DC bus with neutral point capacitor. Same concept can be used with three legs to generate three phase output where sharing of the DC-bus is possible (Panagis P *et al*, 2008). As the number of voltage level goes on increasing the required number of clamping diode & its rating goes on increase. So as voltage levels increase the NPC topology will be impractical due to this fact. The reason for the inverter to have clamping diodes connected in series is so that all diodes can be of the same voltage rating and be able to block the right number of voltage levels. For example, in above figure all diodes are rated for Vdc/4 [VDC/ (m-1) in general] and the D1´ diodes need to block 3Vdc/4 and therefore there are three diodes in series.

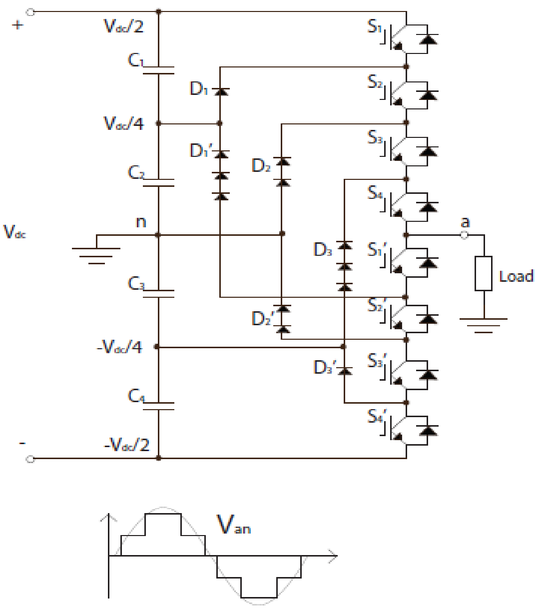

Fig. 3 Multilevel Diode Clamped/Neutral Point Inverter, NPCMLI

However, for low voltage application there is no need to connect components in series to withstand the voltage, since components with sufficient high voltage ratings are easy to find. With this configuration five levels of voltage can be generated between point A and the neutral point n; Vdc/2, Vdc/4, 0,-Vdc/4,-Vdc/2, depending on which switches that are switched on. A waveform from one phase-leg of the inverter can also be seen in above figure in which the steps are clearly visible. As we progress NPCMLI for higher number of voltage levels the steps will be smaller and the waveform more similar to a sinusoidal signal but with a higher number of voltage levels the complexity & number of components goes on increase (Nabae.A *et al*, 1981). To achieve the different voltage levels in the output a setup of switching state combinations are used. Below table different states for the five-level NPC inverter are shown. Note that there is the possibility to only turn on (and off) every switch once per cycle, meaning that the inverter can generate a stepped sinusoidal waveform with a fundamental switching frequency.

Table 1 Firing Sequence of IGBT's

Output Voltage	S_1	S_2	S_3	S_4	S'_1	S'_2	S'_3	S'_4
$\frac{V_{dc}}{2}$	1	1	1	1	0	0	0	0
$\frac{V_{dc}}{4}$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-\frac{V_{dc}}{4}$	0	0	0	1	1	1	1	0
$-\frac{V_{dc}}{2}$	0	0	0	0	1	1	1	1

Table 1 gives us a idea of switching of the devices to achieve the output.1 indicate device is on while 0 indicate device is OFF. it can be seen that for the voltage Vdc/2 all the upper switches are turned on, connecting point a to the Vdc/2 potential, see Figure 3. For the output voltage Vdc/4 switches S_2, S_3, S_4 and S'_1 are turned on and the voltage is held by the help of the surrounding clamping diodes D_1 and D'_1. For voltage levels –Vdc/4 or –Vdc/2 clamping diodes D_2 and D'_2 or D_3 and D'_3 hold the voltage, respectively. For the voltages ±Vdc/2 the current, when both voltage and current are positive (positive current goes out from the inverter), goes through the four top or bottom switches. For the other states positive current, while voltage is positive, goes through the D_x diodes and negative current through the D'_x diodes and also through the switches in between the clamping diodes and the load. For example, for state Vdc/4 positive current goes through diode D1 and switches S2, S3 and S4. If there is a DC-source charging the DC-bus there is also currents flowing through the DC-bus to keep the DC-bus voltage constant. We can see from Table 1 that some switches are use more frequently as compare to the others, mainly S_4 and S'_1.All the voltage level created as long as a sinusoidal output wave that requires the use these voltage levels. During inverter operation i.e.active power transfer to load result in unbalanced capacitors voltages since the capacitors are charged and discharged unequally, partly due to different workloads and that current is drawn from nodes between capacitors. The total DC-bus voltage will be the same but the capacitors voltage will deviate from each other. While transferring real power current is drawn from, for example, capacitor C1 and C2 during different amount of time, as can be seen in the left part of below figure.

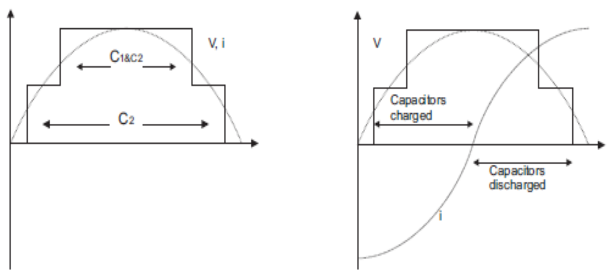

Fig.4 Charging and Discharging cycles of capacitors

The time intervals in the figure 4 represent the discharge time and as can be seen C2 is discharged more, leading to unequal capacitor voltages. Also, during for example the Vdc/2 state current discharges both C1 and C2 but in the Vdc/4 state current is drawn from the point between C1 and C2, discharging C2 but charging C1. This makes the voltages over the capacitors to deviate in a special way. When only transferring reactive power however the NPCMLI does not have this voltage unbalancing problem, see right part of above figure 4. This is because of that time intervals during which the capacitors charged and discharged are equal during reactive power transfer, as the figure 4suggests. To solve the voltage balancing problem an additional balancing circuit can be added or more complex control methods can be implemented.

Demerits

NPCMLI at higher number of voltage levels is unusual due to the capacitor unbalance problem. When it comes to component quantities, such as number of needed components and their ratings, some things have to be considered that have been partially mentioned in the text. As mentioned the inner switches are on more frequently than the outer switches since they are used in several of the switching states. Because of this a different amount of RMS current will follow through the switches depending on their position, with higher current rating needed for the inner switches. Position of the clamping diodes is also important to their ratings since they need to block different levels of reverse voltage depending on where they are connected. If equal ratings are assumed for every individual diode, for every extra level of voltage that needs to be blocked and extra diode is required. This in turn explains why the NPC topology is unpractical with higher amounts of voltage levels since, because of the extra blocking diodes, the number of diodes grows quadratic ally with the level m following the equation (m - 1)* (m- 2). This is however not valid for low voltage inverters, but for high and medium voltage application this is still the case. As for the other components (m- 1) DC-capacitors, 2(m-1) main diodes and 2(m- 1) switches are needed for the NPCMLI topology.

Operational Principles of the Cascaded ML Conventional Inverter

Below figure 5 shows the conventional structure of single phase MLI inverter. It consists of 'n' cells of switch circuits. For cells from '1' to (n-1), each k-cell is composed of one dc voltage source and two switches (Sk1,Sk2); one switch (Sk2) is connected in series with a dc voltage source and the other switch (Sk1) is connected in parallel with both the dc voltage source and the series switch (K.Surya Suresh *et al*, 2012). Based on this configuration, each cell can generate two states (0V) and the dc voltage source associated with the considered cell. Cell 'n' is composed of only the dc source voltage resulting in generating only one state (Vn). As a result, the dc link voltage Vbus has (n-1) states, they are (V1, V2…., Vn), as shown in figure 6.

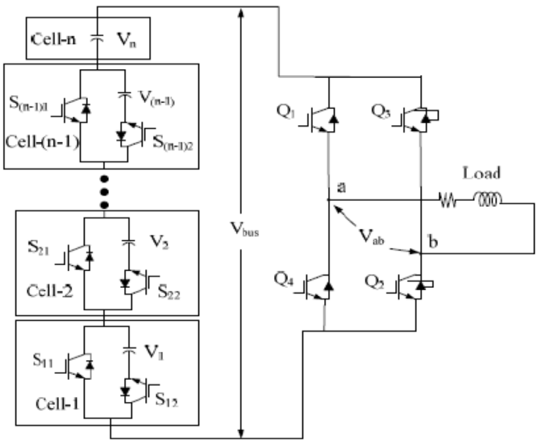

Fig.5 Structure of the conventional cascaded dc link MLI

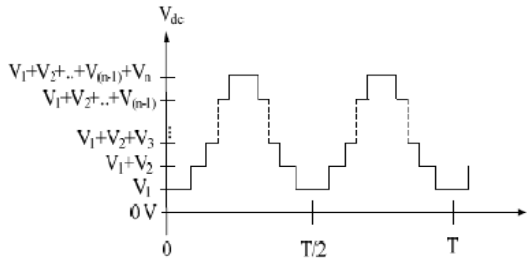

Fig.6 Typical output waveform of Vdc

Single-Phase Five –Level PWM Inverter

In order to generate five levels, the number of the required cascaded cell is n-2. One cell uses two switches with the dc source while the other cell is only the dc source as shown in Fig.7. Assume that the dc voltage sources are equal; V1=V2=Vdc. The dc link bus voltage Vbus will have two states, Vdc or 2Vdc and the load output voltage will have five states 0.5Vdc, Vdc, 0, -Vdc, -0.5Vdc. The zero state can be generated either by switching the upper switches together or the lower switches together (R.Seyezhai *et al*, 2008). The other four states can be generated from the dc bus voltage V bus based on folded cascade unit operation. The below figure shows conventional single-phase five-level inverter diagram.

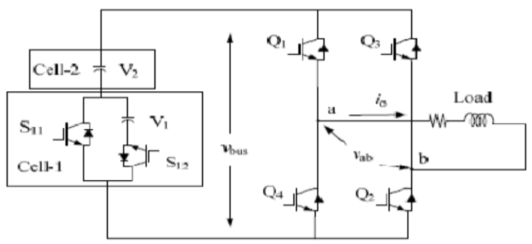

Fig.7 Conventional single-phase Five-level inverter configuration

The operation of the single-phase five-level inverter, employing PWM, can be divided into 10 switching states based on the direction of the output current as given by table 2 below.The signal generation waveforms are generated using one modulating signal and two carriers. The amplitude of the modulating signal is (Ar) and the amplitude of each carrier is (Ac). In addition, each carrier is shifted with the carrier amplitude (Ac) from the former one.

Table 2 Switching States and direction of output current

Switching states	The output voltage (V_{ab})	The Direction of the output current (i_0)	ON states Switches
1	V_{dc}	positive	Q_1, Q_2 and S_{11}
2	V_{dc}	negative	D_1, D_2 and S_{11}
3	$2V_{dc}$	positive	Q_1, Q_2 and S_{12}
4	$2V_{dc}$	negative	D_1, D_2 and S_{12}
5	0	positive	Q_1, D3 or Q_2,D_4
6	0	negative	D_1, Q_3 or D_2,Q_4
7	$-2V_{dc}$	positive	D_3, D_4 and S_{12}
8	$-2V_{dc}$	negative	Q_3, Q_4 and S_{12}
9	$-V_{dc}$	positive	D_3, D_4 and S_{11}
10	$-V_{dc}$	negative	Q_3, Q_4 and S_{11}

The switching strategy used to generate the gate signals is accomplished by comparing the reference signal, which is rectified sinusoidal, with two triangular carrier wave forms having the same frequency and phase angle, but with different offset voltages. When the lower carrier signal is compared with the reference signal, the first level of output voltage will be generated. This means that the modulation index (MI) is less than pre equal 0.5 (50%). The behavior of conventional inverter is similar to the full-bridge three levels PWM inverter. The distribution of the harmonic components in output voltage is similar to that of the conventional inverter having the values of two times the modulation index. The mentioned above is the first operational mode (G. Gopal *et al*, 2013). On the other hand, if the required output voltage is increased beyond the modulation index 0.5, the output will result from comparing the upper carrier signal with the same reference signal. Therefore, the second level of the output voltage will be generated and it will be the second mode. According to the amplitude of the voltage reference, the operational interval of each mode varies within a certain period. Thee modes are determined as the phase angle depends on the modulation index. The output voltage levels, according to the switch ON/OFF conditions, are shown in Table 3.

Table 3 Output voltage levels

V_{ab}	Switching states					
	Q_1	Q_2	Q_3	Q_4	S_{11}	S_{12}
$+V_{dc}$	ON	ON	OFF	OFF	OFF	ON
$+0.5\ V_{dc}$	ON	ON	OFF	OFF	ON	OFF
0	ON	OFF	ON	OFF	OFF	OFF
0	OFF	ON	OFF	ON	OFF	ON
$-0.5\ V_{dc}$	OFF	OFF	ON	ON	ON	OF
$-V_{dc}$	OFF	OFF	ON	ON	OFF	ON

Mode A: $0 < wt < \theta 1$, $\theta 2 < wt < \pi$
Mode B: $\theta 1 < wt < \theta 2$
Mode C: $\pi < wt < \theta 2$, $\theta 4 < wt < 2\pi$
Mode D: $\theta 3 < wt < \theta 4$ (1)

The modulation index MI of the conventional five levels PWM inverter is defined as: $MI = A_M/2A_C$

Where:
AM The peak value of the modulating (sinusoidal) signal,i.e. the voltage reference (Vref).
AC The peak-to-peak value of the carrier (triangular).
The Switching patterns employed in the conventional inverter are illustrated in figure 8. Also, the frequency ratio, mf is defined as $m_f=f_c/f_m$. Where:
fc The frequency of the carrier (triangular) signal.fm The frequency of the modulating (sinusoidal) signal.

Merits of this scheme

Cascaded H-bridge inverter has a modularized layout & because of that problem of the DC link voltage unbalancing does not occur, it is easily expanded to multilevel.

Suitable for higher level DC voltages

Demerits of this scheme: However for this topology large number of switching devices required which equals to 2(K-1) where K is number of levels.

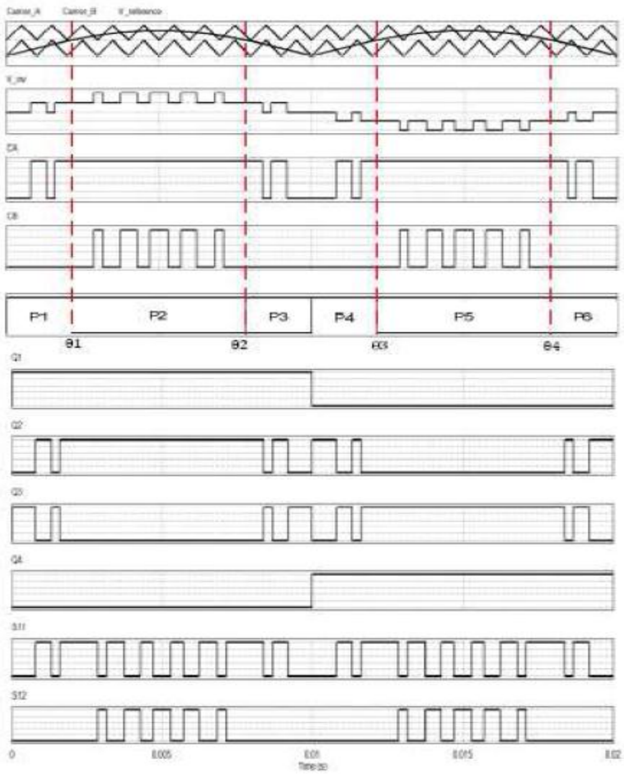

Fig.8 Switching Patterns of the proposed inverter

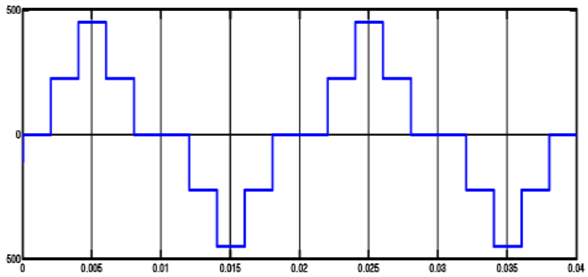

Fig.9 Five level output voltage of conventional five-level multilevel inverter

Conclusion

In this paper we have studied basic two level inverter, further different types of multi-level inverters. In multi-level inverter input DC switch at different potential helps to get the waveform near to fundamental sine wave. This results in reducing cost and size of output filter. Also we have studied different PWM techniques for switching of IGBT's.

References

Siriroj Sirisukprasert, Jih-Sheng Lai and Tian-Hua Liu (August-2002), Optimum harmonic reduction with a wide range of modulation indexes for multilevel converters, *IEEE Transactions on Industrial on Electronics*, Vol.49, Issue 4, pp.875-881.
Lai.J.S, and Peng, F.Z. (May/Jun 1996), Multilevel converter- a new breed of power converters, *IEEE Transactions on Industrial Applications*, vol.32, Issue3. Pp.509-517.
Rodriguez, J.; Jih-Sheng Lai; Fang Zheng Peng (Aug 2002), Multilevel inverters: a survey of topologies, controls, and applications, *Industrial Electronics, IEEE Transactions* on , vol.49, no.4, pp. 724- 738, doi: 10.1109/TIE.2002.801052
Panagis, P., Stergiopoulos, F., Marabeas, P.; Manias, S. (June 2008), Comparison of state of the art multilevel inverters, *Power Electronics Specialists Conference, 2008, PESC 2008, IEEE*, vol., no., pp.4296-4301, 15-19
Nabae.A. Takahashi.I., and Akagi. H. (September/October 1981), A new neutral-point clamped PWM inverter, *IEEE transactions on Industrial Applications*, Vol. IA-17, pp. 518-523.
K.Surya Suresh and M.Vishnu Prasad (2012), Performance and Evaluation of new multilevel inverter topology, *International Journal of Advances in Engineering and Technology*,Vol. 3, Issue 2, pp. 485- 494.
R.Seyezhai and B.L.Mathur (May 2008), Harmonic evaluation of multicarrier PWM techniques for cascaded multilevel inverter, *Proc. 2nd International Conference on Electrical Engineering and its Applications, Algeria, ICEEA 2008*, 20- 21, pp. 3 - 8.
G.Gopal, B.Shankaraiah, M.Chinnalal, K.Lakshmi Ganesh, G.Satyanarayana, D.Sreenivasa Naik (September 2013), A New topology of Single-Phase Seven level Inverter with Less Number of Power Elementsfor Grid Connection, *International Journal of Innovative Technology and Exploring Engineering (IJITEE)* ISSN: 2278-3075, Volume-3, Issue-4