International Journal of Current Engineering and Technology
E-ISSN 2277 – 4106, P-ISSN 2347 – 5161

Available at http://inpressco.com/category/ijcet

Research Article

Study the High performance of Organic semiconductor CuPc Field Effect Transistor

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Accepted 05 May 2015, Available online 10 May 2015, **Vol.5, No.3 (June 2015)**

Abstract

In this paper, the device properties of copper phthalocyanine CuPc p-type semiconductor thin film transistors OTFTs with various gate insulator layer thicknesses SiO_2 has been studied using the MATLAB software program (version7). The operating performance of the OTFTs was found to be depended on the channel length L, channel width w, SiO_2 layer thickness and CuPc active layer thickness. The results show the effect of different SiO_2 layer thicknesses on the organic field-effect transistor OFETs give various performances. OFETs gives high performance at thickness of gate insulator 100nm compared with the SiO_2 layer thicknesses at (200nm, 300nm), where L=0.25mm , w=4.7mm, n-doped Si substrate functions as the gate, and CuPc layer thickness in the range of 50-60nm. This may be attributed the source-drain bias dependence to a significantly trap-affected carrier transport process in a conduction channel formed in the vicinity of the gate insulator. The CuPc OFET carrier mobility of about $1.22x10^{-3}$ $cm^2/V.s$, on/off current ratio of 10^2 and low threshold voltage of (-4V,-3V,-2V) for gate insulator thicknesses (300nm, 200nm, 100nm) respectively were calculated.

Keywords: *CuPc, field-effect transistor, gate insulator.*

Introduction

Since the first article on copper phthalocyanine (CuPc) of de Diesbach and von der Weid in 1927 (R. Zeis *et al* , 2005*)*, extensive research has been carried out on this material. The outstanding chemical stability and strong blue dye properties of CuPc resonate through numerous articles and reviews-several hundred literature references and patents describe the significance of Cupc in science and technology. There are two general forms of phthalocyanine, which is metal free phthalocyanine (H_2Pc) and various metal substituted forms phthalocyanine (Pcs). Metal free Pcs contains two hydrogen atoms in the center of molecule while the various metal Pcs occurred when the hydrogen atoms are replaced by a single metal atom(C.V Abraham and C.S.Menon , 2005). CuPc is a p-type semiconductor and has the advantage of being sufficiently stable towards chemicals and heat treatment (S. Ambily and C.S. Menon , 1999 ; V. Shaji *et al*, 2002). CuPc is also easily available and its advantages are approved by the strong and broad spectral absorption, light fastness and excellent thermal stability (R. Prabakaran *et al*, 2008). Depending on the deposition conditions different molecular orientations and crystalline structures can be obtained. CuPc molecules have a planar structure as shown in Figure (1(a)), and in a crystal they are packed together forming column-like structures (Figure 1(b)).

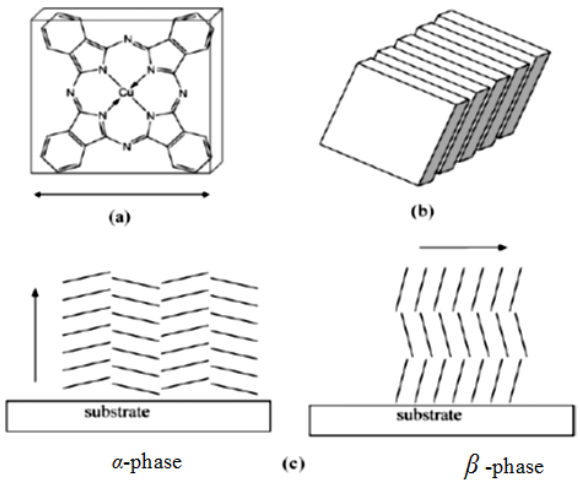

Fig.1 (a) Molecular structure of CuPc, (b) CuPc stacked molecules , (c) α and β CuPc structures.

Two typical crystalline polymorphous structures are usually observed in CuPc material: the well-known metastable *α*- and stable *β*-phases (M. Della Pirriera *et al*, 2009). The main differences between them are the molecular overlapping area (Figure 1(c)). Generally,

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powder CuPc shows the so-called 'β-phase' (a = 19.4 Å, b = 4.8 Å, c = 14.6 Å, β = 120◦*)*. For CuPc thin films deposited on substrate at room temperature, the film grows in the α-phase (a = 25.92 Å, b = 3.79 Å, c = 23.92 Å, β = 90.4◦*)*, whereas the β-phase is obtained for samples deposited or annealed at higher temperature.
Over the past years remarkable progress has been made in the development of thin-film transistors (TFTs) based on organic semiconductors. In several key figures of merit, such as e.g. the on/off current ratio, the field-effect mobility, and the threshold voltage, the best organic TFTs can now compete with commercial amorphous silicon TFTs. The gate dielectric plays a crucial role in this regard. It is responsible for the reliability of the device, governs the required driving voltages and also limits the polarizations which can be achieved at the interface. In organic TFTs the most common dielectric is SiO_2 (F. Roth and M. Huth , 2011) . It is well known and characterized from its use in the conventional semiconductor industry, and has the advantage of chemical stability and excellent insulation with low leakage currents and the dielectric constant is about (3.9)(Liu Xueqiang *et al* , 2010).

In this article, we describe the theoretical study of the device properties of OTFTs based on CuPc, which is a typical p-channel active material (Satoshi Hoshino *et al*, 2002) , in order to highlight the thickness dependence of device operation. We revealed that the device performance of the OTFTs depended on the thickness of the gate insulator layer.

Theory

To define the semiconductor under consideration we will consider the general case of a p-type semiconductor, with holes as majority carriers. In the metal-oxide-semiconductor field-effect transistor (MOSFET), the current is controlled by an electric field applied perpendicular to both the semiconductor surface and the direction of current. The heart of the OFET is the metal organic-oxide-semiconductor capacitor.

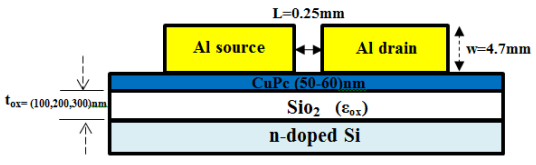

Fig.2 Schematic cross-section of the CuPc OFET

Figure (2) show cross section of p-channel CuPc organic field-effect transistor. The channel length L, channel width W and the oxide thickness t_{ox} are defined on the figure. In the p-channel device, a negative gate- source voltage must be applied to create channel region, of holes that connects the source and drain regions. The threshold voltage denoted as V_T for p-channel device.

In the p-channel device the hole is the charge carrier, rather than the electron, and the conventional current direction and voltage polarities are reversed and the device biased in the nonsaturation region at $V_{SD}<V_{SD(Sat)}$, the drain –source current I_{SD} is given by (Donald A. Neamen , 2010):

$$I_{SD} = K_P[2(V_{SG} + V_T)V_{SD} - V_{SD}^2] \quad (1)$$

Where $V_{SD(Sat)}$ is the source- drain voltage that produces zero inversion, V_{SG} the source- gate voltage. The parameter K_P is the conduction parameter for the p-channel device and is given by:

$$K_P = \frac{W\,\mu C_{OX}}{2L} \quad (2)$$

Where μ is the field effect mobility and C_{ox} is the oxide capacitance per unit area and given by:

$$C_{ox} = \varepsilon_{ox}/t_{ox} \quad (3)$$

The oxide permittivity for SiO_2 $\varepsilon_{ox}=(3.9)(8.85x10^{-14})$f/cm (Liu Xueqiang *et al* , 2010). At $V_{SD}>V_{SD(sat)}$ this region of I_{SD} versus V_{SD} characteristic is referred to the saturation region and the drain current I_{SD} is given by (Donald A. Neamen , 2010):

$$I_{SD} = K_P(V_{SG} + V_T)^2 \quad (4)$$
(for p-channel device)

$$I_{SD} = K_n(V_{SG} - V_T)^2 \quad (5)$$
(for n-channel device)

From eq(4) the $I_{SD}^{1/2}$ is a linear function of V_{SG}. The MATLAB software program has been used to calculate the I-V characteristics and transfer characteristic for CuPc OFET at different thicknesses of gate insulator layer.

Results and discussions

Figure (3) shows the drain- source current characteristics of the CuPc based OTFTs as a function of drain-source bias for gate insulator layer thickness 100nm and various gate voltages. As negative gate bias increased, the current level between drain-source electrodes increased indicating p-type operative characteristics by using eq(1,4) where w=4.7mm and L=0.25mm. It was found that the increase of the drain source current for the gate insulator thickness of 100nm is more than the increase of drain source current for the gate insulator thicknesses of 200nm,300nm at the same gate voltage as shown in figure(4).

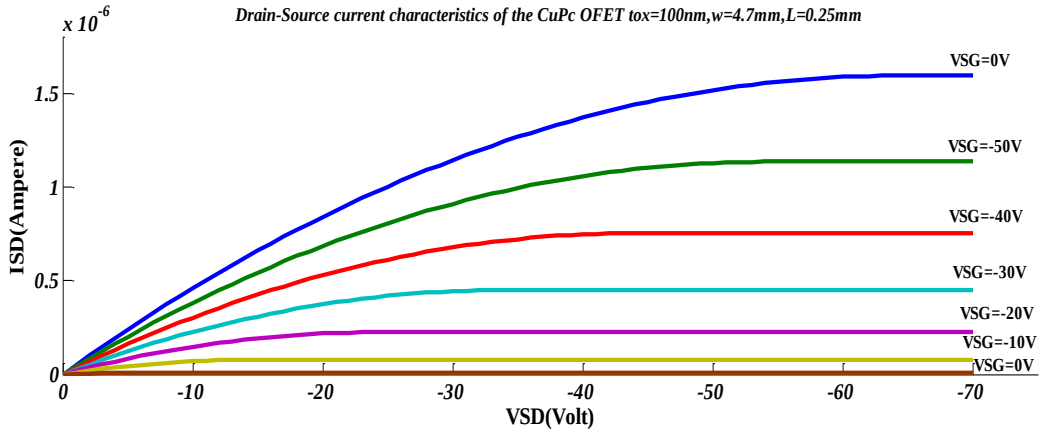

Fig.3 The drain-source current characteristics of CuPc FET with gate insulator thickness100nm

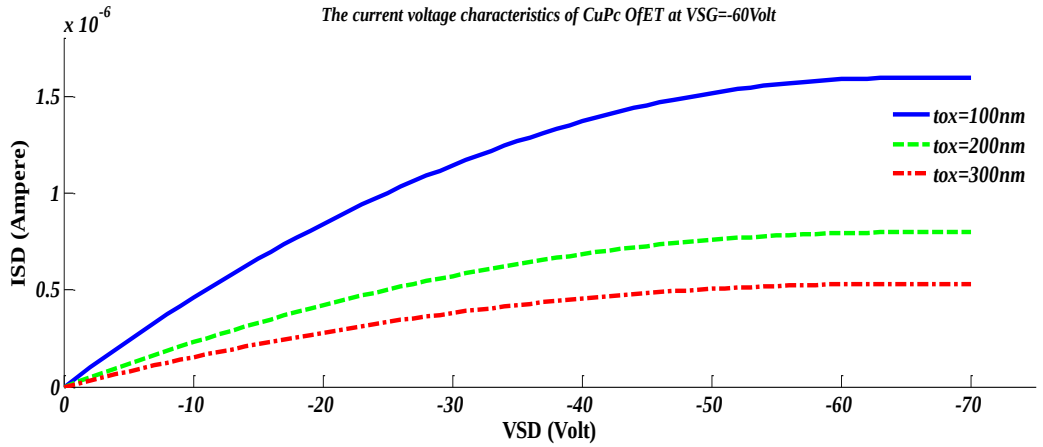

Fig.4 The drain-source current characteristics (at V_{SG}=-60 V) of CuPc OFET with various gate insulator thicknesses of 200nm, 300nm

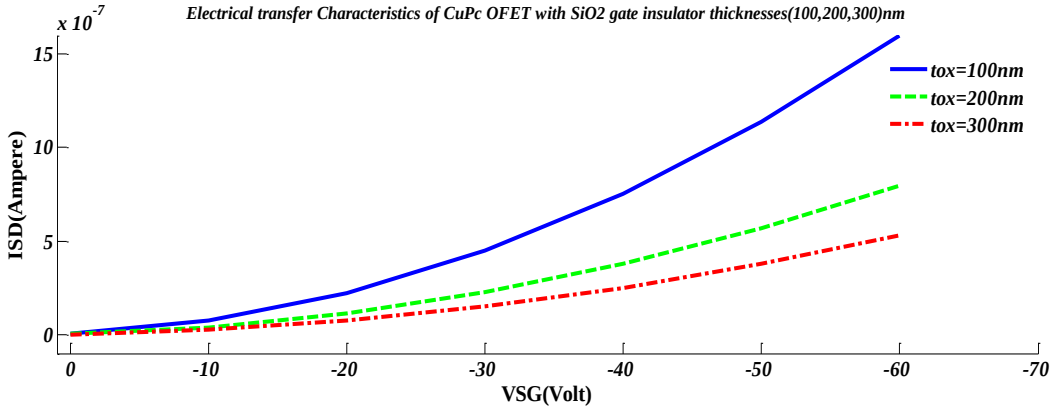

Fig.5 Transfer characteristics of CuPc OFET (at V_{SG}=-60 V) with various gate insulator thicknesses of 200nm, 300nm

It is clear from Figure (4) that the device show high drain-source current at the gate voltage -60V for gate insulator thickness 100nm compared with gate insulator thicknesses of 200nm, 300nm at the same gate voltage.

Figure (5) shows the transfer characteristics of a CuPc based OTFTs for various gate insulator thicknesses and fixed V_{SG}=-60 V. The current on/off ratio was about $\sim 10^2$. These values are in a good agreement with the values presented by other workers (J. Puigdollers *et al*, 2006). The mobility was calculated in the saturation regime which is modulated by eq(4).

Figure (6) shows the plot of $I_D^{1/2}$ versus V_{SG} by using eq (4). From this plot can be used to obtain V_T the extrapolated threshold voltage. The line intercepts the V_{SG} axis at the threshold voltage about ~-4V for t_{ox}

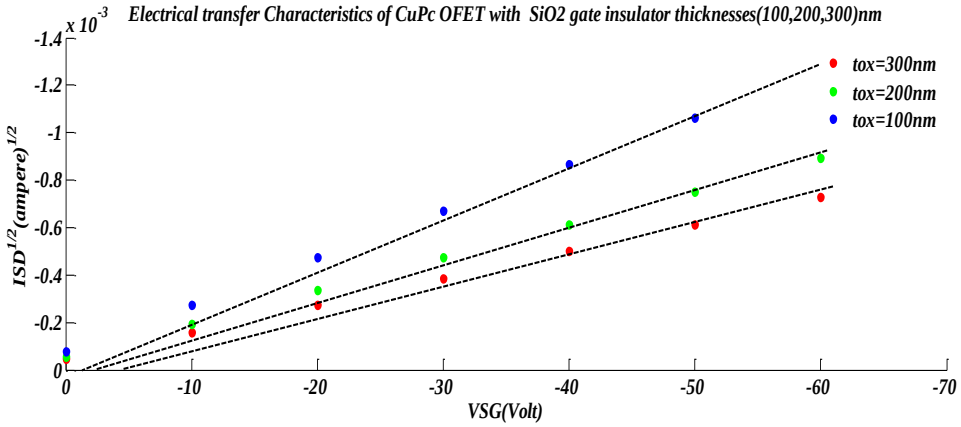

Fig.6 Plot of the square root of drain source current in the saturation regime as a function of the gate voltage for CuPc OFET with various gate insulator thicknesses 100nm, 200nm, 300nm, the straight line is a least-square fit to the points above the 10V. the line intercepts the V_{SG} axis at the threshold voltage(V_T~-4V,-3V,-2V). Its slope is used for determining the field-effect mobility.

=300nm ,-3V for t_{ox} =200nm and -2V for t_{ox} =100nm at V_{SG}=-60 V. Its slope is used for determining the field-effect mobility from eq(4)

$$Slope = \sqrt{\frac{WC_{ox}\mu}{2L}} \quad (5)$$

The field-effect mobility calculated using this method was found to be about ~$1.22x10^{-3}$ $cm^2/V.s$ for various thicknesses.

Conclusion

The outcome of this study can be summarized as follows:

- Copper phthalocyanine based organic thin film transistor at various gate insulator layer thicknesses were studied theoretically using MATLAB software program.
- To enhanced the performance of the device (by increasing the capacitance of the gate insulator , channel width and the mobility of active layer as well as decreasing the channel length, the threshold voltage) the thickness of the gate dielectric has been reduced from 300nm to 100 nm.
- The best device performance was obtained for OTFTs with a gate insulator thickness 100nm and the threshold voltage was reduced from -4V to -2V by reducing the thickness of the gate insulator from 300nm to 100nm.

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