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Research Article

Flexible Divider with Reduced Area and Power

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Abstract

An efficient multiband flexible divider is designed for Bluetooth, Zigbee and other wireless standards and it is implemented using Xilinx ISE 9.1i and modelsim SE 10.0b.It consist of modified multi modulus prescaler and integrated P & S counter. The proposed system will have low power and area compared to existing system

Keywords: *Flexible Divider, Zigbee, Bluetooth etc.*

1. Introduction

In recent trends the feature size of the MOSFET'S is continuously shrinks. This attracts the research and development of low power radio frequency CMOS integrated circuits. In case of mobile wireless-communication, low power operation are of crucial importance as the battery lifetime is limited by the power consumption. Low power also helps to reduce the operating temperature and results in stable performance. In last few years various wireless standards have been developed for various applications.

To achieve low power, division operations were performed using hardware module divider. Since they were not convenient to use, synchronous techniques came to practice. In synchronous technique the presence of clock signal may cause clock skew and dynamic power consumption. To overcome this disadvantage asynchronous techniques are used instead of synchronous.

In order to minimize the manufacture cost silicon wafers are used. The step size of the fractional-N synthesizer is reduced because of reference frequency. So frequency divider (FD) or prescaler are used to support multi standard application. The function of the prescaler is to generate a signal whose frequency is a fraction of input frequency. The prescaler operates at high frequency and power consumption is high. There are three types of frequency divider they are given below

1) Flip-flop based frequency divider.
2) Regeneration frequency divider.
3) Phase-locked loop frequency divider.

Usually synthesizer consists of voltage controlled oscillator (VCO). Some type of synthesizer will also use counter. The synthesizer can be an integer-N type with programmable counter. The integer can also be called as integer frequency divider or fractional-N type synthesizer.

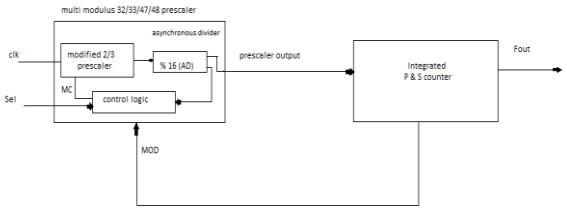

Fig 1 Multiband flexible divider

2. Wideband E-TSPC 2/3 Prescaler

The extended true single-phase clock (E-TSPC) 2/3 prescaler operates at higher frequency and consumes more power where TSPC 2/3 Prescaler operates at low frequency and consumes low power. To overcome this problem a wideband single-phase clock 2/3 prescaler is used in this design. The extended wideband single-phase clock 2/3 prescaler consist of flip-flop and NOR gates.

Modified prescaler replaces the NOR gate with PMOs switch and bubbled AND gate. The bubbled AND gate doesn't require any additional transistors. When MC =1 the PMOS switch is opened and prescaler operates at divide-by 2 mode. When MC =0 the PMOS switch is closed that allows the out of flip-flop1 to flow through bubbled AND gate and operates at divide-by 3 mode. While operating in divide-by 2 mode only flip-flop2 is ON thus saving half of the power.

*Corresponsing author **S.Preskovia** is a P.G.Scholar, II M.E VLSI Design and **P.Vigneswari** is working as Assistant Professor

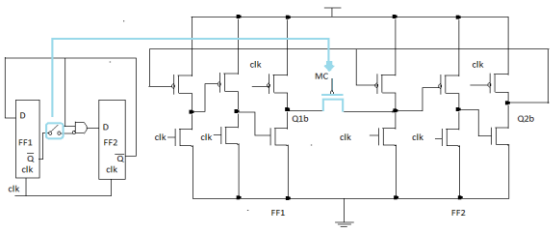

Fig 2 Wideband single-phase clock 2/3 prescaler

3. Multimodulus 32/33/47/48 Prescaler

The multimodulus prescaler consist of 2/3 prescaler block with asynchronous divider, 2:1 mux and logic gates. This prescaler is capable of dividing frequency by 32,33,47,48. They reduce the complexity of multiband divider and save the power consumption. Depending upon the sel signal the prescaler decides to divide the frequency by 32/33 or by 47/48.

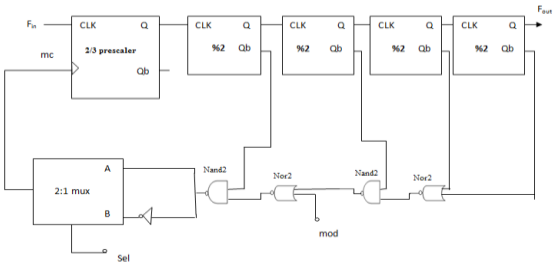

Fig 3 Multi modulus 32/33/47/48 prescaler

A. Case 1: sel = '0'

Sel is given as control signal to 2:1 mux. The two inputs of mux are A and B, where A is the direct output driven from NAND2 gate and B is the inverted output of NAND2 gate. When sel=0 the mux select the input A and give it to the input of 2/3 prescaler. The multi modulus prescaler operates as 32/33 prescaler.MOD is the logic signal that controls division ratio.

When MOD=1 then output of NAND2 gate is logical '1' and MC ='1' the prescaler operates as divide-by-2 mode.

The division ratio N is

$$\mathbf{N = (AD * N_1) + (0 * (N1 + 1)) = 32}$$

Where N1 = 2 and AD = 16 prescaler operates as divide-by-3 mode. If
MOD = 0, then MC is logically '1' for 30 input clock cycles thus prescaler operates at divide-by-2 mode and mc is logically '0' for remaining 3 clock cycles.
The division ratio N+1 is

$$\mathbf{N + 1 = ((AD - 1) * N_1) + (1 * (N1 + 1)) = 33}$$

B. Case 2: Sel = '1'

When sel = 1 the mux select the input b and give it to the input of 2/3 prescaler. The multi modulus prescaler operates as 47/48 prescaler.

When MC = '1' the prescaler operates ad divide-by-3 mode.
When MOD = '1' the division ratio N+1 is

$$\mathbf{N+1 = (AD * (N_1 + 1)) + (0 * N_1) = 48}$$

If MOD='0' the division ratio N is

$$\mathbf{N = ((AD - 1) * (N_1 + 1)) + (1 * N_1) = 47}$$

4. Integrated P & S Counter

They consist of integrated P & S counter with AND and XNOR logic gates. S counter has 6 bit cells (C_0, C_1, C_2, C_3, C_4 and C_5) and P counter consist of 7 bit cells (P_0, P_1, P_2, P_3 , P_4 , P_5 and P_6). The values for S counter are assigned and P counter starts to count until it reaches the value of S counter. Once it reaches then the output of XNOR gate will be set '1' else the output of XNOR will be '0'. Now all output of XNOR(X_1, X_2, X_3, X_4, X_5 and X_6) is given to AND gate. If P_6 is logical '1' then it is given as input to AND2 gate along with output of AND1 gate. If the output of AND2 gate is logically '1' then MOD signal is set. If P_6 is logical '0' then it is given to Reset the MOD signal.

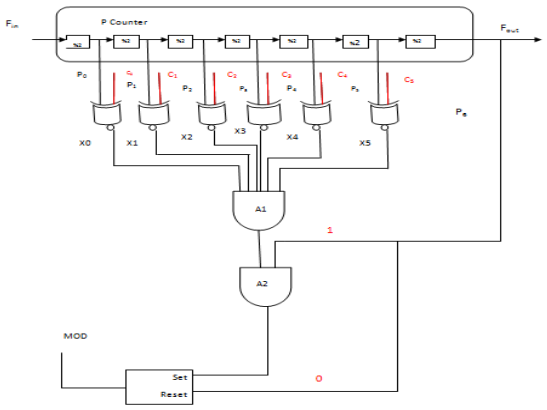

Fig 4 Integrated S & P counter

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		19
Vccint 1.20V:	5	6
Vccaux 2.50V:	7	18
Vcco25 2.50V:	0	0
Clocks:	0	0
Inputs:	0	0
Logic:	0	0
Outputs:		
Vcco25	0	0
Signals:	0	0
Quiescent Vccint 1.20V:	5	6
Quiescent Vccaux 2.50V:	7	18

Conclusion

In this paper, a modified 2/3 prescaler and integrated P & S counter makes the circuit simple. The circuit simplicity path and reduced power consumption. Post layout simulation result proved its advantage in power, speed and layout area against previous designs.

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