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Research Article

Multiple Word Length Optimization based algorithm and architecture for low power QPSK base band receiver

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Abstract

The necessity of low power VLSI circuits in wireless communication applications is increasing with high pace. In wireless communication IC design, research on power optimization methods by reducing the word-lengths in digital implementation of algorithms is gaining importance. The optimum word length selection for each signal in an algorithm is crucial for Word length optimization (WLO). In this paper, we present an algorithm for optimal Multiple Word-Length (MWL) computation at every signal stage in base band receiver using system level parameters. The word length, which is sufficient to carry signals with minimum acceptable Signal to Quantization Noise Ratio (SQNR) is computed at every stage and applied to a scalable Register Transfer Level (RTL) design. The Power optimized RTL model is simulated and the resulted SER values are compared with theoretical values. At each optimization, level area and power analysis are also carried out. Xilinx tools are used for timing and power analysis. The optimized architecture demonstrates a power saving of 40% for Es/No = 8 dB, in comparison to the 16-bit Uniform Word Length (UWL) based design for Zynq 7Z020 device based receiver. The bit accurate simulation results show less than 2 dB variation with the theoretical SER curves for different input SNR values at input. The results demonstrate a promising direction of VLSI optimization based on SNR requirement and MWL technique in Wireless Communication applications.

Categories and Subject Descriptors: *Low power VLSI, Digital Signal Processing.*
General Terms*: Low power VLSI Design, Word Length Optimization (WLO), Signal to Quantization Noise Ratio (SQNR)*
Additional Key Words and Phrases*: Dynamic range, fixed point, scaling in DSP systems*

1. Introduction to WLO

Present day mobile communication and wireless products are based on low power Very Large Scale Integration (VLSI) techniques. The research over last few decades in the device and circuit design techniques resulted a wide category of wireless and battery powered applications. The future mobile communication system related algorithms are complex and require great efforts to optimize for low power. To meet the next generation low power demands, the designers are exploring algorithm level and architecture level techniques. The Word Length Optimization (WLO) based techniques are promising and being attempted by several researchers. Unlike in processor architecture kind of design, the possibility of selecting suitable word-length in communication and signal processing applications provides an opportunity for speed, area and power optimization (David Maliniak, 2010; Alivelu Manga, N *et al*, 2014; George Constantinides *et al*, 2004)

The power optimization techniques at device and circuit level are being used in majority of 28 nano meter ASICs and FPGAs (Peiyi Zhao, 2009). The scope for power optimization at higher levels of abstraction is the new challenge in low power communication system design. As per the survey given in (David Maliniak, 2010) the scope of low power optimization is limited to 10% for Gate and Layout level techniques, whereas architecture level redesign can yield 90% power optimization.

The WLO algorithms fall in category of architecture level optimization as they enable designer to scale the architecture to result in low power circuits. In addition to power optimization, the reduced word lengths can result in high speed data path. Due to these low power and high speed advantages this optimization technique has more importance in communication and DSP architectures. The research work presented here proposes an algorithm for multiple word length (MWL) based WLO, and applies it to QPSK base band receiver architecture.

2. Existing WLO Approches

The Word Length Optimization (WLO) problem is traditionally considered as, the selection of bit widths based on the interval growths after each arithmetic operation of data path .This section attempts to formulate

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the problem of WLO and also presents the existing approaches. Several researchers contributed to the WLO in different dimensions. Total existing literature pertaining to WLO can be classified into two categories. One category of articles emphasizes on formal approach for WLO, which can be applied to a large class of DSP systems. The second category of articles discusses WLO, in the context of a specific architecture based on features specific to that algorithm. In this paper we ignore the second category of work, and focus on formal methods as they become suitable for integrating in Electronic Design Autiomation (EDA) tools. This research focuses on evolving a generic optimization algorithm, which can be applied to all categories of DSP datapaths where SNR is one of the parameter deciding system performance.

While analyzing the WLO in DSP algorithms, the linear and non-linear classification is studied in detail by several researchers (George Constantinides *et al*, 2004). Handling the non-linear architectures resulting with adaptive and recursive DSP algorithms is considered as the complex part in applying WLO techniques (Alivelu Manga, N *et al*, 2014) The WLO methods can be classified into two categories.

(1) Analytical methods

(2) Simulation based approach

The analytical methods utilize selected analytical properties of the operations comprising the given algorithm (Gabriel *et al*, 2008). Analytical methods usually result in more conservative word lengths, as they use worst case ranges and error models of operators in a design. They are often faster and can guarantee a lower bound for the error. However these methods directly cannot result in optimal hardware. The simulation based methods simulate the design with a set of input stimuli and track the minimum and maximum values attained by each signal in the data path. Based on these values the suitable word length can be computed. This leads to designs that are close to the optimum (Constantinides, G.A. 2003) but no error bound can be guaranteed. If the tight word lengths are selected based on simulation, then overflows may occur. Hence usually additional few bits will be considered for deciding the worst case signal values. This is the popular method used in the transformation of algorithm (Tor M. Aamodt *et al*, 2008) from DSP to ASIC.

A computation graph G (V, S) consisting V set of graph nodes, each representing an atomic computation or input/output port. The S ⊂ V ×V is a set of directed edges representing the data flow (George Constantinides *et al*, 2004). This notation is also referred as data flow graph (DFG). The nodes in DFG contain a specific value of in and out degrees representing the input and output ports of the node.

As the DSP requires both positive and negative numbers, signed representation is required in representing each S. A two's complement signal $j \in S$ of computation graph $G(V, S)$, has two parameters n_j and q_j , as illustrated in Fig. 1. The parameter n_j represents the total number of bits in the representation of the signal (including the sign bit), and the parameter q_j represents the number of bits occupied from right for representing the fractional part. Depending on the nature of signal even the $q_j > n_j$, indicating the binary point could be present outside the represented bits (George Constantinides *et al*, 2004; NI)

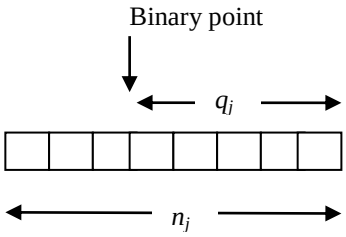


Fig. 1 Signal $j \in S$ of computation graph G (V, S)

An algorithm given at (NI) minimizes the hardware resources of fixed-point operations for a given accuracy constraints

3. QPSK Digital Base Band Receiver

The present radio, broadcast and mobile communication systems are built around the principles and architectures of Software Defined Radio (SDR). In SDR design approach major receiver functionalities are built with software approach. The software can be realized with combination of Hardware Description Languages (HDL) or program languages such as C and C++. However the frequency translation from pass band to base band usually achieved by analog stages. In super heterodyne approach by employing single or multiple frequency translation stages, the signal is converted from radio frequency (RF) band to intermediate frequency (IF) band. In SDR systems signal is digitized at this stage by using ADC with required sampling rate. The frequency conversion from IF to base band is performed by Digital Down Converter (DDC) to produce I and Q components. In the present research the DDC output, complex (I + j Q) signal is considered as input for the base band receiver (Alivelu Manga, N *et al*, 2014).

In current mobile standards, popularly used digital modulation schemes are Phase Shift Keying (PSK) and Quadrature Amplitude Modulation (QAM) variants. Both of these two come under linear modulation category, which can be represented in quadrature form as given in Equation (1) (Alivelu Manga, N *et al*, 2014).

$$s(t) = I(t)\cos(2\pi f_0 t) - Q(t)\sin(2\pi f_0 t) \quad (1)$$

Equation (1) represents the general form of input to the base band receiver, where I and Q correspond to inphase and Quadrature phase values. The COS and SIN components are resultant of carrier residue, which will be removed in carrier recovery stage. Optimization principles while processing base band I and Q components which are applicable to one linear modulation type are also applicable to all other variants. Considering these aspects, the QPSK base band receiver architecture is considered for illustrating the proposed optimization method in Fig.2 (Nikita Patel *et al*, 2014).

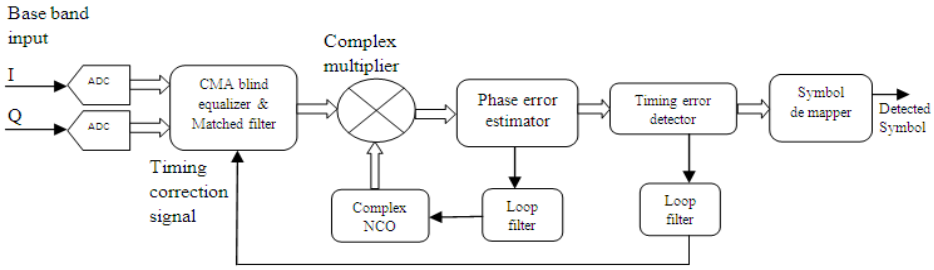


Fig. 2 High Level Architecture of Digital Base Band Receiver for QPSK

The general architecture of High Level Architecture of QPSK receiver can be seen in the Fig. 2. The I and Q components out of DDC are given to the CMA (Constant Modulus Algorithm) equalizer and then the output is complex multiplied with NCO(Numerically Controlled Oscillator) and phase error estimation is performed with inverse tan function implemented with look up table. The loop filter for phase correction and timing correction consists of Proportional-Integral (PI) loop control. The proportion term and integral term gains can be modified at run time, by using external ports of RTL modules,he the output is given to a Timing Error Detector (TED) is then to symbol demapper givig out the bits which are transmitted.

The CMA is stochastic gradient-descent type, which adjusts the equalizer filter coefficients in the direction of the negative gradient. The algorithm can be defined as given in equation (2). Where μ is the step size, ∇_W is the gradient with respect to the equalizer tap coefficients, J is the cost function of the algorithm, and e(n) is the error signal of the algorithm, while (.)* denotes complex conjugation. The iterative computations of filter coefficients w(n+1) is obtained from previous cycle coefficient values w(n).

$$w(n+1) = w(n) + \mu (\nabla_W J)$$

$$= w(n) + \mu\, e(n)x^*(n) \qquad (2)$$

As the e and x are complex, this equation will have real and imaginary components.

For locking on to the carrier of a received modulated signal, the phase locked loop plays a critical role in a communication system. In an ideal communication system the transmitted carrier frequency is known and we need to calculate its phase offset for accurate demodulation. Due to imperfections in the transmitter, the actual carrier frequency may be slightly different than the expected frequency (Tiwari, B.B *et al*, 2005). We can model the difference between the actual and expected carrier frequencies as a time varying phase. A Phase locked looping system can track this time varying phase, if the frequency mismatch is small relative to the carrier frequency (Tomasi 2004).

Zero Crossing Timing Error Detector (ZCTED) uses the zero crossings that occur when adjacent symbols cause a zero crossing in the MF outputs, called transition. Due to the symmetry of the pulses used in communications, when sampling the MF output at a rate of two samples per symbol and every other symbol is a zero crossing, the middle sample is at the correct timing instant. For a Zero Crossing Timing Error Detector (ZCTED) to function, it first requires a transition in the symbols with an associated zero-crossing. No transition results in a timing error calculation of zero.

3.1 Signal Characteristics - Dynamic Range and SNR

In a typical communication system the distance between receiver and transmitter can range anywhere between, few meters to few hundreds of kilometers. The input signal received is very large when the receiver is close to transmitter and very small when it is far. Hence number representation with high dynamic range is required. Typically 80 dB dynamic range is processed in communication receivers. A practical ADC of 16 bit is used for this purpose in receiver digital front end.

As the channel is noisy, the signal available at receiver has noise energy mixed in it. In a typical receiver chain there are several stages of amplification and frequency translation. The signal to noise ratio (SNR) available at receiver decides the performance of communication system. The blocks in receiver chain either improve the SNR or reduce. Usually amplifiers, mixers and attenuators which are found in receiver front end reduce the SNR, which is accounted through noise figure. As a result, the signal at ADC output in receivers has high dynamic range (hence higher word length) but less SNR.

The dynamic range of a system is the ratio of the maximum signal power (P_{max})to minimum signal power(P_{min}) that is of interest (Tomasi, 2004). The dynamic range determines the signal levels over which the receiver needs to be sensitive for processing the signal. As this number is larger in value usually it is expressed in dB scale as given in Equation (3)

$$\text{Dynamic Range (DR) } in\ dB\ scale = log_{10}\left(\frac{P_{max}}{P_{min}}\right) \qquad (3)$$

Usually the ADCs are designed to accept input with certain dynamic range and produce output as binary words. The input analog circuit which performs signal conditioning (amplification or attenuation and adding offset) decides the true power level over which the ADC can function. The number of ADC bits decides the granularity level at which the analog voltage can be measured. The resolution defines the smallest signal change that can be measured. The accuracy with which the analog to digital conversion takes place is decided by the resolution. The values of accuracy and dynamic range can

be either computed in voltage levels or in power scale by considering the input impedance of ADC (which is 50Ω or 75Ω in most of the cases).

For a given application, the signal processing requirements demand a certain dynamic range and accuracy. The number of bits selected from ADC bits and further word lengths in every stage of processing need to consider these requirements, while achieving the optimization. This dynamic range is generally smaller than the total dynamic range offered by system. As the system is supposed to accept input right from lowest power level to highest power level, the system level dynamic range is higher (Alivelu Manga, N *et al*, 2014).

Taking the ratio of root mean square (RMS) value of full scale input to RMS value of quantization noise and all other harmonics the resultant maximum Signal to noise (SNR) ratio can be given through the Equation (4), where N is the number of ADC output bits and q is the quantization step size.

$$\text{SNR(dB)} = 20\log\frac{\text{rms signal}}{\text{rms noise}} =$$

$$20\log\left(\frac{\left(2^{N-1}\times\frac{q}{\sqrt{2}}\right)}{\frac{q}{\sqrt{12}}}\right) = 6.02N + 1.76 \text{ dB} \quad (4)$$

This implies that the SQNR increases approximately 6dB fro every bit aided to the word length.

3.2 Performance of Digital Demodulator – SER and EVM

A symbol can be described as either with a specific weight given to I and Q terms at base band level. The I and Q when multiplied with COS and –SIN at the desired carrier frequency results in pass band signal.

'**SER**' stands for Symbol Error Rate. It is also an average figure used to describe the performance of a digital transmission scheme. It is defined as the ratio of total number of symbols detected erroneously in the demodulator and the total number of symbols received by the receiver over a fairly large session of information transmission. Again it is assumed that the same number of symbols is received as it has been transmitted by the modulator. For QPSK, the symbol error probability P_s is related to the bit error probability P_b by (N I, 2012).

$$P_s = 2P_b - P_b^2 \quad (5)$$

All Other parameters which are also related to the performance of a digital system can be calculated from the below equations.

i) E_b/N_o

The ratio of bit energy per symbol to noise power spectral density (**E_b/N_o).**

We can calculate E_b/N_o for QPSK from P_b using the formula (N I, 11).

The bit error probability (P_b) is related to the Q function as

$$P_b = Q\left(\sqrt{\frac{2E_b}{N_0}}\right) \quad (6)$$

Where Q(x) is a Gaussian integral function or Q-function

$$Q(x) = \int_x^\infty \frac{1}{2\pi} e^{-u^2} du \quad (7)$$

ii) E_s/N_0

The ratio of signal energy per symbol to noise power spectral density (**E_s/N_0)** for QPSK can be calculated as in Equations (8), (9) (Proakis *et al*, 2001)

$$E_s / N_0 = 10\hat{}(E_s / N_0 + 10) * k \quad (8)$$

$$E_s / N_0 = E_b / N_0 + 10\log_{10}(k) \text{ (in dB)} \quad (9)$$

Where k=no of bits/symbol which is 2 for QPSK

iii) SNR

Signal power to Noise power can be calculated from Equation (10)

$$SNR = E_s / N_0 * \left(T_{samp} / T_{sym}\right) \quad (10)$$

Where T_{samp} is sampling period and T_{sym} is the symbol period. In the present implementation one sample per symbol is used for detection hence the Es/No and SNR are used alternatively.

Error vector Magnitude (**EVM)** is defined as T, the root-mean-square (RMS) of the error between the measured symbols and the ideal ones i.e., e=$\underline{w}$–$\underline{v}$ as shown in Fig. 3 (N I, 2012)

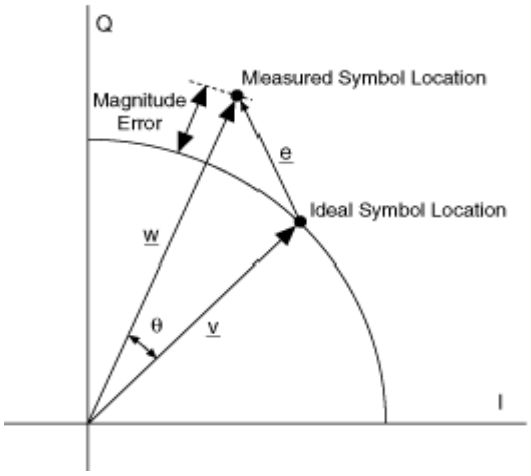


Fig. 3 Graphical Representation of EVM

Where $\underline{v}$ is the ideal symbol vector
$\underline{w}$ is the measured symbol vector
$\underline{v}$ is the magnitude error
Θ is the phase error
$\underline{e}$=$\underline{w}$-$\underline{v}$ is the error vector
$\underline{e}$/$\underline{v}$ is EVM

EVM over a measurement window of N symbols is defined as in equation (11)

$$EVM = \frac{\sqrt{\frac{1}{N}\sum_{j=1}^{N}\left[(I_j - \tilde{I}_j)^2 + (Q_j - \tilde{Q}_j)^2\right]}}{|v_{max}|} \quad (11)$$

Where I_j is the *I* component of *J-th* symbol received. The SNR can be recalculated from EVM as per equation (12)

$$SNR \triangleq \frac{1}{EVM^2} \quad (12)$$

4. Scope of Power Optimization

The paper at (David Maliniak, Feb 2010),) presents relationship between EVM, BER and SNR for several digital modulation schemes. The paper considers the fact that for digital demodulators, which are sampled at data rate the E_s/N_o directly represents SNR. Where E_s is symbol energy and $N_o/2$ gives the noise power spectral density. The figure 4 shows the BER values for various SNR values under this condition. The E_s/N_o values required for achieving Bit Error Rate (BER) less than 10^{-5} for various digital modulation schemes are taken from figure 4 and given in Table 1

Table 1 Es/No values required for BER less than 10^{-5}

Modulation scheme	Approximate SNR (Es/No) required
BPSK	9.5 dB
4 – QAM	12.5 dB
16 – QAM	19 dB
64 – QAM	25.5 dB

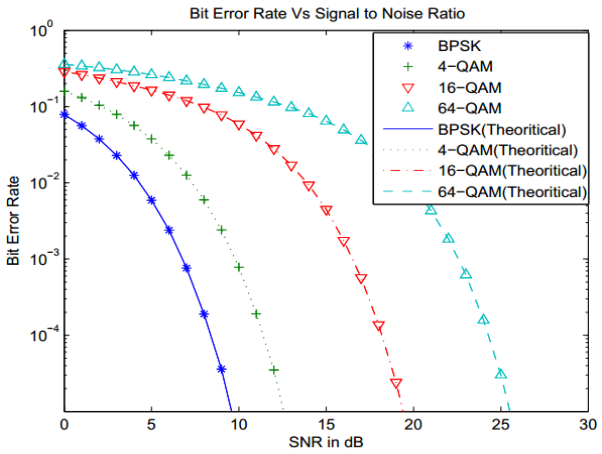


Fig. 4 BER Vs SNR for Various Digital Modulation Schemes

4.1 SQNR and Accuracy constraints based WLO

In the algorithm development stage floating point data types are used to represent signal values at all stages. In the RTL implementation stage fixed point data types are usually preferred to satisfy the cost and power consumption constraints. Only few scientific computations and associated algorithms require the dynamic range of floating point representation and cannot be implemented with fixed point numbers. Most of the signal processing algorithms used in communication applications can be implemented with fixed point representation (Constantinides, G.A. 2003; Tor M. Aamodt *et al*, 2008; E. Sedano *et al*, 2012; T. E. Schmuland *et al*, 2012). The two system level performance aspects accuracy and dynamic range are directly affected by the selected signal representation mechanism.

The choice of signal representation and word length selection, is a non-trivial problem in the present day in low power and high performance demanding type wireless communication architectures.

The Word Length Optimization (WLO) problem is traditionally considered as, the selection of bit widths based on the interval growths after each arithmetic operation of data path. The word length allocated at each signal stage directly affects two parameters; maximum representable value and accuracy (Slosman *et al*, 2013). None of the existing techniques explains how to adopt the WLO for different category of signal processing modules based on system level end performance constraints. The presented solution here in the context of communication receiver applications uses maximum desired SNR of signal as end performance criteria. The presented algorithm computes word lengths at each stage based on the maximum achievable SNR. To establish proof of proposed algorithm a scalable architecture for base band QPSK receiver is used.

The proposed algorithm considers the computational graph as general form for representation of given VLSI implementation of signal processing algorithm. The quantization noise resulting with bit truncation is considered along with noise present in signal to define signal to Quantization Noise Ratio (SQNR)**.** The proposed approach uses SQNR as the basic metric to decide the required number of bits at each signal stage. From the system level specification, such as expected symbol error rate (SER) the final output signal stage SQNR is computed. From output stage the WLO algorithm back traverses to compute SQNR after each node. The node contribution to the increase or decrease in SQNR is pre-computed in the form of processing gains. From the SQNR values at each stage the word length is computed. All the word lengths in the forward paths of the receiver are computed with this method (Satyam Dwivedi *et al* 2012; Daniel Menard *et al* 2012)

The recursive paths are present in equalizer and timing error adjustment blocks. Considering the maximum equalization requirements, the word length of coefficient's is pre-computed. Based on this the processing gains of even these recursive blocks are made available for the WLO algorithm. Similarly considering the worst case timing error detection requirements, the word lengths in these paths are decided. With these approaches the circular dependencies of the recursive paths are resolved (Slosman *et al* 2012).

4.1.1 Specified Algorithm Description

Algorithm: Multiple word length (MWL) based algorithm

Input: Data Flow Graph G(V, S), and required performance factors of total system (CNR, SNR, DR,

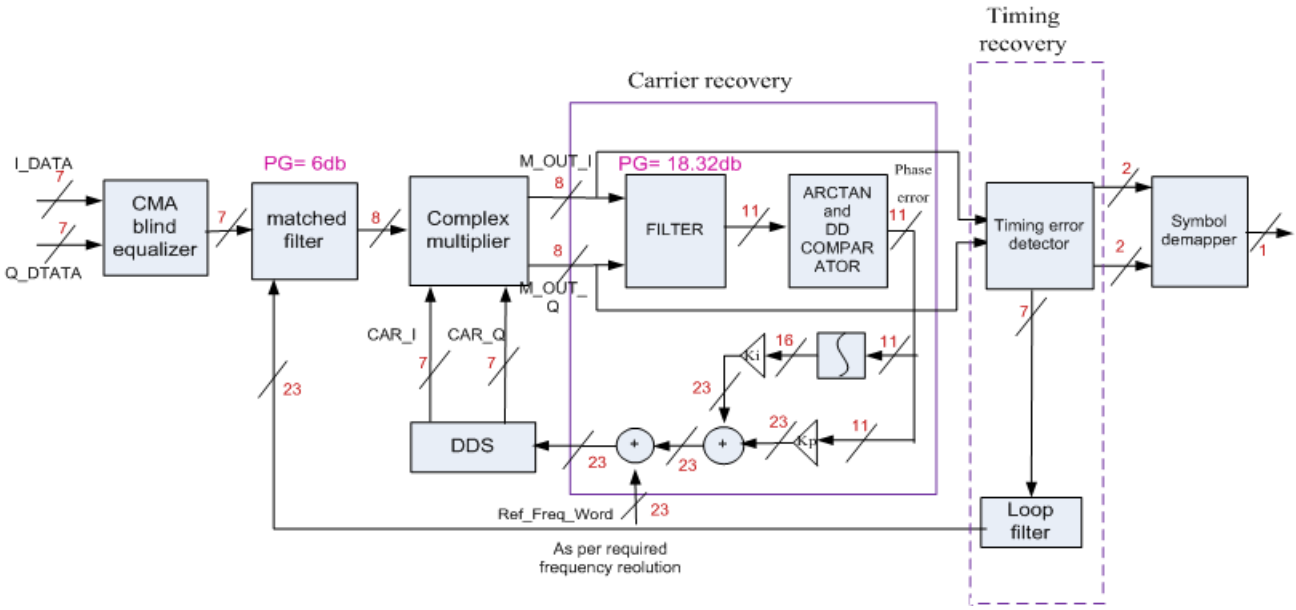


Fig. 5 Base Band Receiver Optimized For Input Signal 40 dB SNR

Table 2 Optimized bit widths

Stage	Bit widths (without sign bit)				Sélection criteria
	No optimization in data path (UWL)	For Es/No = 35 dB	For Es/No = 12 dB	For Es/No = 8 dB	
Input to CMA eqalizer	15	7	4	3	Required SNR at input.
Matched filter input	15	7	4	3	Matched filter offers 10.9 dB processing gain
Matched filter output	15	7	6	5	Matched filter offers 10.9 dB processing
Complex multiplier output	15	9	6	5	
Low pass filter output	15	10	7	6	Matched filter offers 9 dB processing gain
ARC TAN output	15	10	7	6	No gain is added here
Integrator output	23	16	10	9	Integrator adds some amount of gain.
Frequency word	23	24	23	23	Selected based on frequency resolution
Input to timing error loop filter	15	11	5	4	Based on the TED used
Input to symbol demapper	15	2	2	2	For QPSK all the 4 symbols can be represented throgh 2 bits
Output of symbol demapper	1	1	1	1	As the output is always a bit either ‘0’ or ‘1’

BER, SER). Also the tables for performance factors link up to implementation parameters (Es/No Vs SER)

Output: Word length values at each signal $j \in S$ (n_j, q_j)

INITIALIZE : initial processing gain = 0, n_j to maximum value
FOR EACH i = $V_i \rightarrow V_o$ (INPUT NODE $V_i \rightarrow$ OUTPUT NODE V_o)

IF RECURSIVE // such as adaptive filter

Processing Gain $PG_i = PG_{i-1} + MAX\_EXPECTED\_PG_V$

ELSE

Processing Gain $PG_i = PG_{i-1} + PG_V$

END

END

FOR EACH i = $V_o \rightarrow V_i$ (OUTPUT NODE $V_o \rightarrow$ INPUT NODE V_i)

$SQNR_o$ = f (required system level performance aspects at output) // Compute SQNR at output node

INITIALIZE : $WL_o = SQNR2BIT(SQNR_o)$

WHILE V_i ~= input node // until we reach input node

$SQNR_i = SQNR_{i+1} - PG_{Vi}$

$WL_i = SQNR2BIT(SQNR_i)$

END

END

V= nodes in datapath
S= signals in datapath
CNR=Carrier to Noise Ratio
SNR=Signal to Noise Ratio
DR=Dynamic Range
Es/No=Energy per symbol to Noise power spectral density ratio.

Considering most of the wireless applications maximum SNR of 35 dB is considered for simulation. Also considering the minimum SNR requirement of 8 dB in 802.16 wireless standard ,simulation results are presented. in next section.

The modified block diagram of a base band receiver considering all the optimization bit width can be seen in Fig. 5 it shows the datapath for 35 dB input signal SNR. The stages where the filter offers processing gain are labeled in diagram. The minimum accuracy constraints of frequency resolution and time resolution, the frequency word and timing control word are considered as 24 bit.
This design is considered as datapath with capability in handling highest SNR of 35 dB. The table below lists the MWL calculated at each stage for different targeted SNR conditions. In the Table 2 additional one bit is considered at each stage to avoid saturation of signed numbers when arithmetic Operations are performed.

5. Simulation and Synthesis Results

5.1 Matlab Simulation – Es/No vs SER validation

The MATLAB simulation of bit truncated model of developed QPSK base band architecture is carried out and results are observed. The figures 6 and 7 show Es/No Vs SER variation for the MWL optimization applied architectures for 3 and 4 bit input datapaths respectively.
For Es/No =8 dB

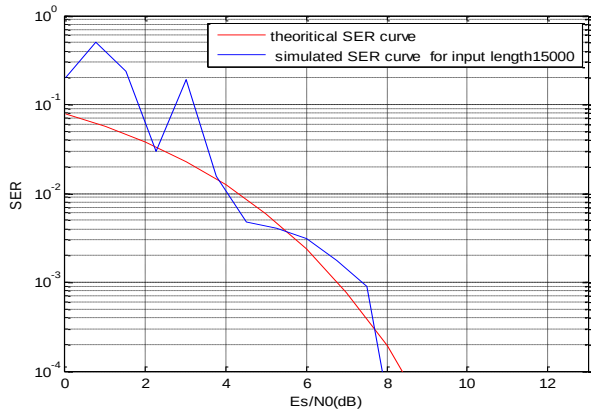


Fig. 6 SER of the MWL optimized (input width 3 bits) receiver compared with the theoretical SER curve

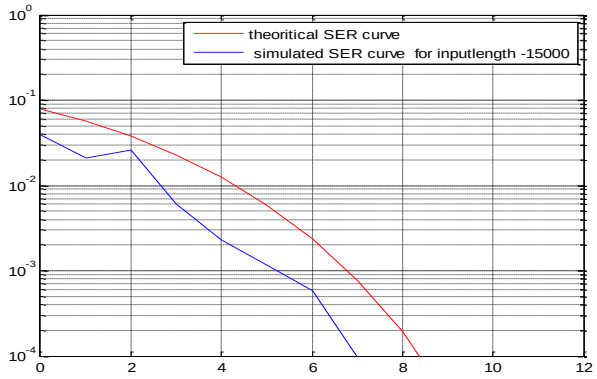


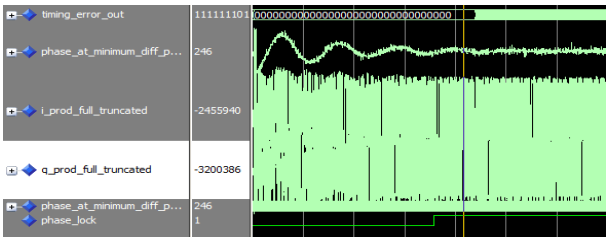
Fig. 7 SER of the MWL optimized (input width 4 bits) receiver compared with the theoretical SER curve

The input to the MWL optimized model is simulated by adding AWGN and multipath fading to achieve the desired Es/No value in steps of 1 dB and SER values are recorded. From above results, it can be concluded that the optimized design is able to perform in comparison with theoretical limit with in 2 dB of error.

5.2 VHDL Simulation Results and Power analysis

The functional validation of the design is carried out using Modelsim simulator. Required test signals are generated from MATLAB, with required noise level and fading introduced.

The performance of carrier recovery loop for frequency offset correction and symbol timing correction is verified in results. The figure 8(a) shows the locking of frequency correction loop when input frequency error is 20 KHz. The figure 8(b) shows the timing recovery to achieve the timing lock when the input symbol range has 5% error. The part b in both figures is zoomed figure in time scale to show the I and Q signal changes.



(a)

(b)

Fig. 8 Frequency loop tracking error 20 KHz (a) showing the phase lock (b) zoomed figure in time domain to show the I and Q after phase lock.

Table 3 Performance, Resource usage and power comparison

Signal condition	Resource and power comparison		
	Parameter	value	comparison
Without optimization	Maximum sample rate	21 Msps	
	Area - slices	17214	
	Area – DSP48	186	
	Power	752 mW	
Word length optimized for SNR = 35 dB	Maximum sample rate	24 Msps	14% improvement in speed
	Area - slices	14240	17 % saving
	Area – DSP48	165	11% saving
	Power	624 mW	17% power saving
Word length optimized for SNR= 12 dB	Maximum sample rate	35 Msps	40% improvement in speed
	Area - slices	10230	40% saving
	Area – DSP48	125	32% saving
	Power	587 mW	22% power saving
Word length optimized for SNR = 8 dB	Maximum sample rate	42 Msps	200% improvement in speed
	Area - slices	9600	44% saving
	Area – DSP48	103	45% saving
	Power	443 mW	40% power saving

The Xilinx 7 series Zynq XC7Z020 FPGA is considered for synthesis and power analysis. The Xilinx Xpower analysis tool is used to analyze the design for power analysis. Table 3 has comparison for four different word length optimization settings.

The power reported for un-optimized design is 752 mW with 16 bit data paths. Whereas for Es/No of 35 dB case results in power dissipation of 624 mW. This can be considered as maximum signal quality requirement in wireless application. Whereas after optimization for Es/No 12 dB the power reported is 587mW. In the full optimization case for Es/No 8 dB, the power reported is only 443mW. This shows 40% power saving when compared to normal design, with uniform word length based approach consisting 16 bit data paths. The increase in speed is resultant due to reduced word lengths and corresponding combinational logic's critical path delays.

Conclusion

A method and algorithm based on word length optimization and communication system performance aspects are presented for wireless base band digital receiver. The architecture consists of blind adaptive equalizer with constant modulus algorithm, with recursive data paths in it. The proposed algorithm demonstrates the multiple word length based optimization for both direct and recursive type data paths. The MATLAB and Modelsim tools are used for simulation and symbol error rate analysis. The Xilinx's ISE tool suite is used for synthesis and power analysis. The 7-series Zynq SOC is used for benchmarking the performance of the proposed method. Peak power optimization of 40% is reported for Es/No = 8 dB, in comparison to the normal design. The SER results match with less than 2 dB error with theoretical results. The demonstrated method shows promising direction of low power optimization of wireless receiver design which can be used in mobile communications, wireless sensor networks and other VLSI implementation of signal processing algorithms.

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