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Review Article

# A Literature Survey on Power Factor Correction using EMI Filter and Boost Converter

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***Abstract***

*This paper presents the study of power factor correction using boost converter: Comparing with the traditional PFC, the proposed PFC has lower requirements of power device ratings, which leads to lower cost, higher efficiency, and lower electromagnetic interference.*

***Keyword:*** *Power factor correction (PFC), electromagnetic compatibility (EMC), single-phase boosts converter, interleaved converters*

## 1. Introduction

Power factor correction (PFC) converters have been widely used in ac–dc power conversions to achieve high input power factor (PF) and low harmonic distortion. However, it works in continuous current mode the switches operate at hard switching and the diodes suffer reverse recovery.

The boost converter is the most widely used topology for achieving PFC. Fig.1 shows a PFC boost converter. The bulk energy storage capacitor sits on the output side of the boost converter rather than just after the diode rectifier bridge. The average inductor current (in each high-frequency switching cycle), which charges the bulk capacitor, is controlled to be proportional to the utility line-voltage waveform. For proper operation, the output voltage must be higher than the peak value of the line voltage and the current drawn from the line at any given instant must be proportional to the line voltage.(Paul Nosike Ekemezie *et al* 2014)

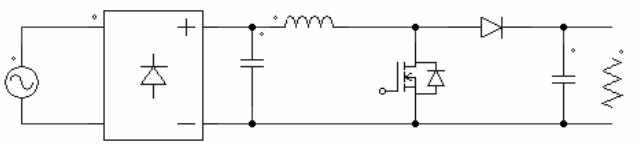

**Figure1:** Boost PFC ac-dc converter

In order to maintain good EMI performance and reduced switch current ratings, the PFC boost converter is usually operated in the continuous conduction mode (CCM). However, operating the boost converter in the CCM causes increased stress on the boost diode. While the boost transistor is off, load current flows through the boost diode. When the transistor turns on, the diode must recover quickly to prevent the output capacitor from discharging into the transistor. The diode has a finite reverse recovery time, $t_{rr}$, during which time it experiences reverse current through and reverse voltage across it. This leads to increased power dissipation in the diode. Using faster diodes helps to reduce diode power dissipation; however, hard turn-off of the diode also increases EMI and degrades diode reliability.

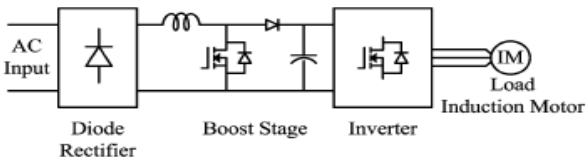


**Figure2:** Traditional power factor correction

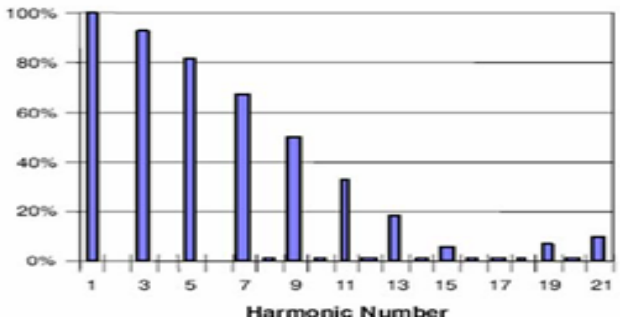


**Figure3:** Harmonic contents of the current waveform in Figure 2

Fig.2 shows the most common approach to signal-phase active PFC, where a boost circuit with an additional filter inductor is used to shape the line current. The boost stage

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forces the dc bus current to follow the line voltage, which results in a nearly sinusoidal line current without phase difference. However, it brings in high dc bus stress, high switching device ratings, high switching losses, and high electromagnetic interference (EMI).(Zhiguo Pan *et al* 2007)

In this paper, a new compact, low-weight, low-cost PFC using a series active filter is proposed. Comparing with the traditional PFC, it has lower device ratings, lower cost, lower EMI, and higher efficiency. The inductor needed in the proposed series PFC is also much smaller than those in the traditional PFC, and in the most cases, the line impedance of the utility line is enough for its normal operation. A hysteresis control strategy, which is simple and easy to implement, is presented to eliminate line harmonics. Simulation and experimental results are given to verify the analysis and demonstrate the control performance.

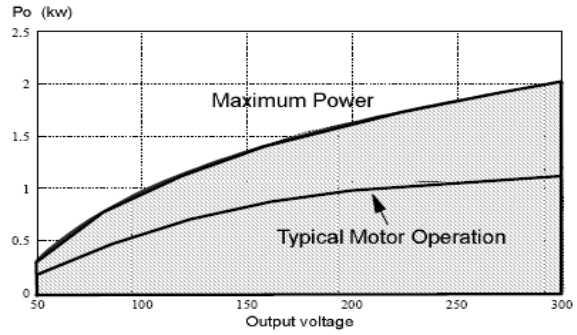


**Figure 4:** Load characteristics of the PFC circuit

*Factor*

Power factor is defined as the cosine of the angle between voltage and current in an ac circuit. There is generally a phase difference Ø between voltage and current in an ac circuit. "Cos Ø" is called the **power factor** of the circuit. If the circuit is inductive, the current lags behind the voltage and power factor is referred to as lagging. However, in a capacitive circuit, current leads the voltage and the power factor is said to be leading.
In a circuit, for an input voltage V and a line current I,
VIcos Ø –the active or real power in watts or kW.

VIsin Ø- the reactive power in VAR or kVAR.

VI- the apparent power in VA or kVA.

Power Factor gives a measure of how effective the real power utilization of the system is. It is a measure of distortion of the line voltage and the line current and the phase shift between them.

Power Factor=Real Power (Average)/Apparent power

Where, the apparent power is defined as the product of rms value of voltage and current. Real power (watts) produces real work; this is the energy transfer component. Reactive power is the power required to produce the magnetic fields (lost power) to enable the real work to be done, where apparent power is considered the total power that the power company supplies. This total power is the power supplied through the power mains to produce the required amount of real power.

If the current and voltage both are sinusoidal in nature and in phase, the power factor is 1.0. If both are sinusoidal but not in phase, the power factor is the cosine of the phase angle. In elementary courses in electricity, this is sometimes taught as the definition of the power factor, but it applies only in the special case, where both the current and voltage are pure sine waves. This occurs when the load is composed of resistive, capacitive and inductive elements and all are linear (invariant with current and voltage).

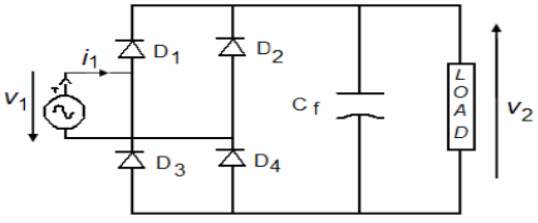


**Figure 5:** Diode bridge rectifier

Switched-mode power supplies present non-linear impedance to the mains, as a result of the input circuitry. The input circuit usually consists of a half-wave or full-wave rectifier followed by a storage capacitor (similar to **Fig. 4**). The capacitor maintains voltage of approximately the peak voltage of the input sine wave until the next peak comes along to recharge it. In this case, current is drawn from the input only at the peaks of the input waveform, and this pulse of current must contain enough energy to sustain the load until the next peak. This is done by dumping a large charge into the capacitor during a short time, after which the capacitor slowly discharges the energy into the load until the cycle repeats. It is not unusual for the current pulse of 10% to 20% of the cycle duration, meaning that the current during the pulse must be 5 to 10 times of the average current as illustrated by **fig.5**. **Fig.3** shows the harmonic content of the current waveform. The fundamental (in this case 50 Hz) is shown with the reference amplitude of 100%, and the higher harmonics are then given with their amplitudes (shown as percentages of the fundamental amplitude). Note that, the even harmonics are barely visible; this is a result of the symmetry of the waveform. The power factor of this power supply is approximately 0.6.

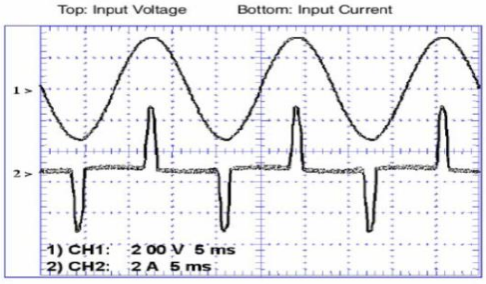


**Figure 6**: Input Characteristics of a typical switched-mode power supply without PFC

Assuming an ideal sinusoidal input voltage source, the power factor can be expressed as the product of the distortion factor and the displacement factor, as given by equation (3). The distortion factor $K_d$, is the ratio of the fundamental root mean- square (RMS) current ($I_{rms(1))}$ to the total RMS current ($I_{rms}$). The displacement factor $K_\theta$ is the cosine of the displacement angle (φ) between the fundamental input current and the input voltage.

For sinusoidal voltage and non sinusoidal current, equation (1) can be expressed as:

$$PF = \frac{V_{rms} I_{1,rms} \cos\varphi}{V_{rms} I_{rms}} = \frac{I_{1,rms}}{I_{rms}} \cos\varphi = K_d \cos\varphi \quad (2)$$

$$PF = K_d K_\theta \quad (3)$$

The distortion factor $K_d$ is given by the following equation:

$$K_d = I_{rms(1)} / I_{rms} \quad (4)$$

The displacement factor Kθ is given by the following equation:

$$K_\theta = \cos\varphi \quad (5)$$

The displacement factor $K_\theta$ can be made unity with a capacitor or inductor, but making the distortion factor $K_d$ unity is more difficult. When a converter has less than unity power factor, it means that the converter absorbs apparent power higher than the active power. This means that the power source has a higher VA rating than what the load needs. In addition, the harmonic currents generated by the converter in the power source affects other equipment.

*Power Factor vs. Harmonic Reduction*

The following equations link total harmonic distortion to power factor.

$$THD\ (\%) = 100 \times \sqrt{\frac{1}{K_d^2} - 1} \quad (6)$$

$$K_d = \frac{1}{\sqrt{1 + \left(\frac{THD(\%)}{100}\right)^2}} \quad (7)$$

Therefore, when the fundamental component of the input current is in phase with the input voltage, $K_\theta = 1$. Then we have,

$$PF = K_d K_\theta = K_d \quad (8)$$

Then:

$$PF = \frac{1}{\sqrt{1 + \left(\frac{THD(\%)}{100}\right)^2}} \quad (9)$$

The purpose of the power factor correction circuit is to minimize the input current distortion and make the current in phase with the voltage.

When the power factor is not equal to 1, the current waveform does not follow the voltage waveform. This result not only in power losses, but may also cause harmonics that travel down the neutral line and disrupt other devices connected to the line.

*Sources of Poor PF*

- Poor power factor caused by reactive linear circuit elements results as the current either leads or lags the voltage, depending on whether the load looks capacitive or inductive.
- Less than acceptable power factor typically associated with electronic power conversion equipment is caused by nonlinear circuit elements.

In most off-line power supplies, the AC-DC front end consists of a bridge rectifier followed by a large filter capacitor (Roma Dash *et al* 2011).

## 2. Types of Power factor Correctors

### *2.1 Passive PFC*

Harmonic current can be controlled in the simplest way by using a filter that passes current only at line frequency (50 or 60 Hz).Harmonic currents are suppressed and the non-linear device looks like a linear load. Power factor can be improved by using capacitors and inductors i.e. passive devices. Such filters with passive devices are called passive filters.

Disadvantage: They require large value high current inductors which are expensive and bulky. A passive PFC circuit requires only a few components to increase efficiency, but they are large due to operating at the line power frequency (Roma Dash *et al* 2011).

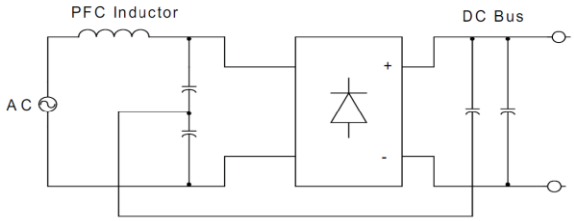


**Figure 7:** A passive PFC circuit

### *3.2 Active PFC*

An active approach is the most effective way to correct power factor of electronic supplies. Here, we place a boost converter between the bridge rectifier and the main input capacitors. The converter tries to maintain a constant DC output bus voltage and draws a current that is in phase with and at the same frequency as the line voltage. .(Roma Dash *et al* 2011)

## 3. Power Factor Correction Circuits

The classification of single-phase PFC topologies is shown in **Fig. 8**. The diode bridge rectifier has no sinusoidal line current. This is because most loads require a supply voltage $V_2$ with low ripple, which is obtained by using a correspondingly large capacitance of the output capacitor $C_f$. Consequently, the conduction intervals of the rectifier

diodes are short and the line current consists of narrow pulses with an important harmonic contents. There are several methods to reduce the harmonic contents of the line current in single-phase system.

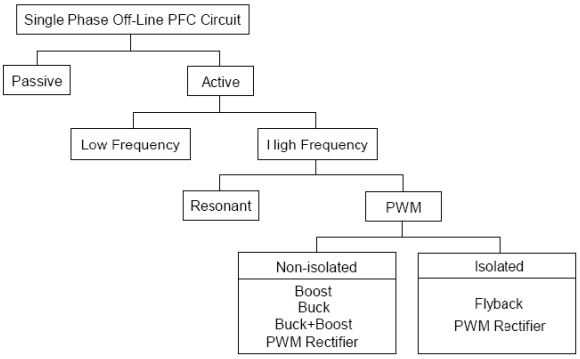


**Figure 8:** Classification of single-phase PFC topologies

## 4. Literature Survey

Use of series active filter is a low-cost approach to power factor correction (PFC). Comparing with the traditional PFC, the proposed PFC has lower requirements of power device ratings, which leads to lower cost, higher efficiency, and lower electromagnetic interference. It also can eliminate the bulky inductor needed in the traditional PFC ( Zhiguo Pan *et al* 2007).

The need to keep EMI emissions by electronic power supplies below the limit specified by international standards have dictated that any new power supply design must include active power factor correction at the front end. The modern trend in power supply designs is towards digital control. The power factor correction circuit employs zero voltage transition arrangement to minimize switching losses. Interface requirements between the power converter stage and the digital control processor are tackled. Average current mode control method is employed in the controller. The complete design has been tested by means of Power Sim power electronics simulation software. The resulting input voltage and current waveforms show that the design is successful. (Paul Nosike Ekemezie *et al* 2014)

The work initially involves simulation of basic power electronic circuits and the analysis of the current and voltage waveforms. It starts with simple circuits with a gradual increase in complexity by inclusion of new components and their subsequent effect on the current and voltage waveforms. We focus on the objective of improving the input current waveform i.e. making it sinusoidal by tuning the circuits. The new analytical method simplifies the design of S2PFCs by making it possible to compare a large number of different designs from the same viewpoint in order to identify the best topology. Finally, research has enabled us to reduce the total size of the additional inductors that are used by a factor of two to three with respect to previous implementations.

For rectifier circuits with power Jactor correction, boost converters are generally used, and as a result the output voltage becomes limited. To expand the controlled voltage range, buck-boost or Cuk converter types should be utilized. This paper presents a circuit configuration with power factor correction by a third type of' buck boost converter, termed as 'canonical switching cell'. Single-phase power factor correction using a buck boost converter can control the output voltage over a wide range, because it has the ability to step-up and step-down the output voltage. Firstly, this paper compares the mechanisms of the power transmission and the characteristics based on the switching ripple of various converters. Secondly, the canonical switching cell is applied to the single-phase power factor correction. It is proposed that this converter is suitable for power factor correction.( Ms. Kurma Sai Mallika *et al* 2007)

Power factor control is a major role in the improvement of power system stability. Many of the existing systems are expensive and difficult to manufacturer. Nowadays many of the converters have no input power factor correction circuits. The effect of power factor correction circuit is used to eliminate the harmonics present in the system. This type of power factor correction circuit is mostly used in the Switched Reluctance Motor controller drive. Fixed capacitor systems are always leading power factor under at any load conditions. This is unhealthy for installations of power system. The proposed embedded system drive is used to reduce the cost of the equipment and increase the efficiency of the system. Experimental results of the proposed systems are included. It is better choice for effective cost process and energy savings (Kurma Sai Mallika *et al* 2007).

When the input current waveform is chosen properly, power factor reduction leads to a reduction in filter capacitor size (and therefore to reduced system cost) while still meeting power quality requirements. Notice that the choice of waveform is independent of the particular power conversion topology to be used. It applies equally to boost, flyback, buck, and other topologies that have been used in PFC applications. (O. Garcia *et al* 2001)

## 5. Problem Formulation

The system to be designed consists of a boost PFC frontend converter plus an AC side EMI filter, as shown in the schematics of Fig. 9.

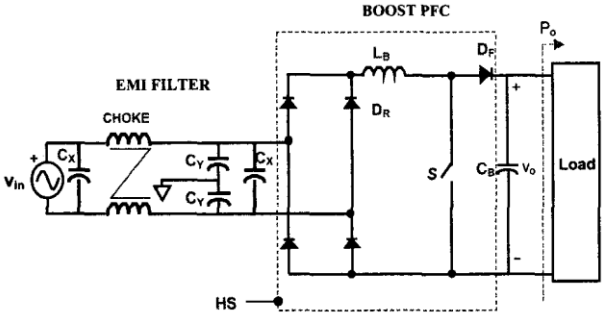


**Figure 9:** EMI filter and Boost PFC stage schematic

The system cost must be minimized while considering the following magnitudes as specifications for the design: output power **(Po),** input voltage range **(Vin-max),** line

frequency, maximum value of the output voltage **(v),** ambient temperature, and maximum temperature of the heat sink. The design must also meet the corresponding PFC and EMI standards.

The term "power factor" or PF in the field of power supplies is slightly deviate from the traditional usage of the term, which applied to reactive AC loads, such as motors powered from the AC power line. Here, the current drawn by the motor would be displaced in phase with respect to the voltage. The resulting power being drawn would have a very large reactive component and little power is actually used for producing work. However, in power electronics field, some of that equipment generates pulsating currents to the utility grids with poor power quality at high harmonics contents that adversely affect other users (Mohan et al. 2005). The situation has drawn the attention of regulatory bodies around the world. Governments are tightening the regulations and setting new specifications for low harmonic current.

Since the number of electronic appliances is growing, an increasing amount of non-sinusoidal current is drawn from the distribution network (Mohan, et al. 2005). Consequently, due to the increasing amount of harmonic currents drawn, the distribution network becomes more and more polluted. As a direct consequence, available power from the grid becomes less. This is because unnecessary current components, which contribute to the root mean square (RMS) value of the line current is drawn from the grid which produces unnecessary power. On the other hand, the harmonic currents distort the line voltage waveform, and may cause malfunction in sensitive electrical equipment connected to the grid.

## 6. Objectives

The Active Power Factor Correction (APFC) is a method to improve the power factor near to unity, reduces harmonics distortion noticeably and automatically corrects the distorted line current of an SMPS. It will replace the Passive Power Factor Correction (PPFC) which has become a conventional method for the past 20 years. This research aims to implement the Unity Power Factor (UPF) for single-phase rectifier which is used in designing the high-end SMPS by using APFC approach. For this purpose, a power electronic circuit is inserted between the bridge rectifier, the output filter capacitor and the load. This approach requires additional semiconductor switches and control electronics, but permits cheaper and smaller passive components. The goals of this research are:

• To simulate and analyze the typical power supplies.
• To investigate the effects of harmonics and low power factor to the power system.
• To simulate and analyze the methodology chosen for UPF.
• To determine the best control mode for UPF.
• To implement a single-phase UPF rectifier in designing the better SMPS.

In this thesis, three types of converters are considered and they were designed in two stages converter. The first stage deals with a rectification process that is AC to DC conversion together with PFC Boost topology while the second stage deals with DC to DC conversion as Flyback topology was used. The preferable type of PFC is Active Power Factor Correction (APFC) since it provides more efficient power frequency. An active PFC uses a circuit to correct power factor and able to generate a theoretical power factor near to unity. Active Power Factor Correction also markedly diminishes total harmonics, automatically corrects AC input voltage, and capable for a wide range of input voltage.

## 7. Methodology

The constant-frequency average-current-mode control for continuous-current-mode operation was chosen as the control strategy for the switch. The output capacitor CB and the average value of the output voltage (v,) are determined independently considering v , - ~ , the maximum peak value of the input voltage (Vin-,-,,) and controller tolerances. The highest average value of the output voltage is **368** V. The highest value represents the worst case. For the implementation of the common-mode choke, it was decided to choose among commercially available designs. The core shape **of** the boost inductor **LB** was considered to be toroidal and the core material was selected. For the viability of the application of a continuous variable optimization approach, all devices (rectifier diodes **DRY** fast diode DF, and controlled switch **S**) were fixed. The cheapest devices meeting the requirements of the system under study were chosen. In particular, for the controlled switch S, an IGBT with an external anti-parallel diode was selected. However, other analyses considering a MOSFET have been performed. **A** single heat sink for all devices was considered. **A** final simplification is made by assuming the layout to be footed throughout the design process. The parasitic shown in **Fig. 2** are estimated according to the layout and component characteristics of the common-mode choke and boost inductor. This is required information for the accuracy in the estimation of the EM1 levels in the LISN resistors to be compared with the standard limit.

### Power Stage Design

The specifications of the boost PFC ac-dc converter are as follows:

AC Input Voltage (rms) 90 V – 270 V
Input Line Frequency 47-63 Hz

Target Efficiency 92% min @ 90VAC / 1000 W

Selection of the boost converter components is carried out following standard procedure, especially as described in. PF is assumed to be 0.99 or greater at low line.

$$P_{in(max)} = \frac{P_{o(MAX)}}{\eta_{MIN}} = \frac{1000W}{0.92} = 1087W$$

$$I_{in(rms)max} = \frac{P_{in(max\ )}}{V_{in(rms)min}} = \frac{1087W}{90V} = 12.1A$$

$I_{in(rms)max} = I_{in(rms)max} = 12.1\times \sqrt{2} = 17.1A$

$I_{in(avg)max} = \frac{2I_{in(pk)max}}{\pi} = \frac{2\times 17.1A}{\pi} = 10.9A$

*A. High Frequency Input Capacitor*

$C_{in} = K\Delta I_L \frac{I_{in(rms)max}}{2\pi\times f_{sw}\times r\times V_{in(rms)min}}$

Where:

$K_{\Delta IL}$ = Inductor current ripple factor (20% in this design)

r = maximum high frequency voltage ripple factor ($\Delta V_{in}/V_{in}$), typically between 3% – 9%, 6% used for this design

$f_{sw}$ =115200Hz is the switching frequency

$C_{in} = 0.2\times \frac{12.1}{2\pi\times 115200\times 0.06\times 90} = 0.62\mu F$

$C_{in}$ = 680 ηF, 450 V, is selected

*B. Input Inductor*

The inductance required is determined by the amount of switching ripple current that can be tolerated.

$V_{in(pk)min} = \sqrt{2}V_{in(rms)min} = 90\sqrt{2} = 127V$

Peak boost transistor duty cycle,

$D_{pk} = 1 - \frac{V_{in(pk)}}{V_o} = 1 - \frac{127}{400} = 0.6825$

Inductor ripple current,

$\Delta I_{L=} 0.2I_{in(pk)max} = 0.2 \times 17.1 \cong 3.42A$

$\Delta I_L$ is based on the assumption of 20% ripple current.

Peak inductor current,

$I_{L(pk)max} = I_{in(pk)max} + \frac{\Delta I_L}{2} = 17.1 + \frac{3.24}{2} = 18.8A$

$L = \frac{V_{in(pk)min}\times D_{pk}}{f_{sw}\times \Delta I_l} = \frac{127\times 0.6825}{115200\times 3.42} = 220\mu H$

L = 2.2 mH is selected, in order to achieve good dynamic performance.

*C. Output Capacitor*

The value of the output capacitor impacts hold up time and ripple voltage. In this design, the criterion for selection of this capacitor is the amount of tolerable ripple in the output voltage, as described in:

$C_{out} \geq \frac{\frac{P_o}{V_o}}{2\pi f_r\times \Delta V}$

Where, $f_r$ is the frequency of the rectified sine wave (100 Hz— worst case), and ΔV is the desired peak-to-peak output voltage ripple.

$C_{out(min)} = \frac{1000/400}{2\pi\times 100\times 0.03\times 400} = 332\mu F$

Derating the output capacitor value by 20% for tolerance in order to guarantee minimum capacitance requirement is satisfied,

$C_{out} = \frac{C_{out(min)}}{1-\Delta C_{tol}} = \frac{199}{1-0.2} = 415\mu F$

For ease of realization $C_{out}$ = 400μF, 450V, is selected.

*D. Boost Diode*

The boost diode is selected in accordance with the considerations given in equation 2. The International Rectifier 15ETH06 15A, 600V, ultra-fast rectifier is selected for this application. The use of an ultra-fast diode helps to increase overall system efficiency reduces the peak stress of the diode and ZVT transistor.

*E. Boost transistor*

The main MOSFET is chosen according to standard design criteria. The maximum voltage that it must be able to handle is the output voltage $V_o$, with ripple. Thus the main MOSFET must handle more than 412 V. The voltage rating must be sufficient to withstand the full output current at low line voltage, maximum load. Fairchild's FCB20N60 N-Channel MOSFET is selected—rated at 600V, 20A, with ROS(on) = 0.15Ω (25°C), Coss ~ 165pF.

*F. Input Rectifier Diodes*

The maximum voltage that appears across an input bridge diode is the maximum input voltage that is encountered during high line conditions $V_{in(rms)max}$ at input of the converter:

$V_{in(pk)} = \sqrt{2}\, V_{in(rms)max} = 270\sqrt{2} = 382A$

The peak current that flows through them is $I_L$( pk )max 18.8A = . The average current that an input diode must conduct is

$I_{in(avg)max}$ = 10.9A

*G. Auxiliary transistor*

The RMS current seen by the ZVS MOSFET is small. A MOSFET with reduced capacitance and higher on-resistance is required in order to reduce switching losses. Fairchild's FCP7N60 N-Channel MOSFET is selected as the auxiliary switch—rated at 600V, 7A, with ROS(on) = 0.53Ω (25°C), Coss ~ 60pF.

*H. Resonant Inductor*

The resonant inductor is selected according to considerations described in.

$\frac{di}{dt} = \frac{I_{in(max)}}{3.t_{rr}} = \frac{18.8A}{105ns} = \frac{179A}{\mu s}$

$L_r = \frac{V_o}{di/dt} = \frac{400V}{179A/\mu s} = 2.2\ \mu H$

*I. Resonant Capacitor*

The resonant capacitor is sized to ensure a controlled dv/dt

of the main switch. The effective resonant capacitor is the sum of the MOSFET capacitance and the external node capacitance. The FCB20N60 has approximately 165 pF of output capacitance; adding an external capacitance of 680pF across the device is adequate.

*J. Auxiliary diodes*

The same diode (the International Rectifier 15ETH06) is selected for the realization of diodes D2 and D3 in Figure 4.

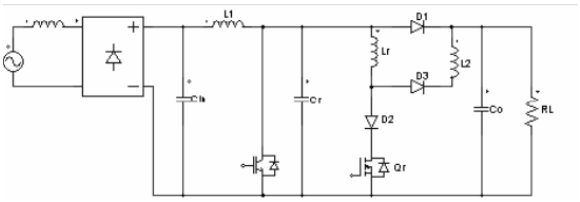


**Figure10:** ZVT boost PFC circuit with additional inductor

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