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Research Article

To Study and Characterisation of N N^+ N Nanowire Transistor (Junctionless) using 2D ATLAS Simulator

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Abstract

A polysilicon gated N N^+ N silicon substrate junctionless nanowire transistor purposed in this paper. Conduction mechanisms in junctionless nanowire transistors (gated resistors) are compared to inversion-mode and accumulation-mode MOS devices uses bulk conduction.The current drive is controlled by dopping concentration concentration. Its characteristics demonstrated and compared with conventional N-MOS transistor using 2D-ATLAS simulator. The result shows that junctionless transistor has a number of desirable features, such as linear variation of I_d with control gate voltage, low leakage current and threshold, effect of different control gate voltage studied and demonstrated in the paper.

Keywords: *N N^+ N transistor (3N), Threshold voltage, Leakage current, Back current, 2D-ATLAS*

1. Introduction

The N N^+ N transistor is a polysilicon gated nanowire transistor with n-type highly doped, drain and source with respect to n-type channel. Junctionless nanowire transistor having highly doped drain and source. Doping concentration is constant and uniform throughout the devices. The device features bulk conduction instead of suface channel conduction. Junctionless transistor is unidirectional,fabrication process is greatly simplified, hot carriers, always ON device there is no doping concentration due to these properties, junctionless transistor can be used in low power application as an always ON &OFF switch.

The conduction of junctinless transistor in ON state a large body current follows through the device due highly doped drain and source and in OFF state device cutoff due to difference of work function substrate and dual gate material.

2. Structure of device and simulation

Structure of N N^+ N junctionless nanowire transistor using following specification is demonstrated in the figure (1).

The structure of junctionless transistor can be design by 2D TCAD simulator (ATHENA deckbuild) and shown in fig (2) These are the structure of purposed device. Structure with electrodes fig (3).

Characteristics

The characteristics of N N^+ N transistor having initial silicon (channel) arsenic doped with doping concentration 1.0E+13. Drain and source doped with concentration 5.0E+15 of arsenic shown as follows

No bias Vg=0V

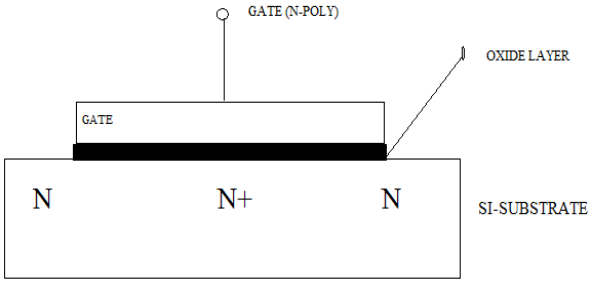

Figure 1: Blok diagram N N^+ N transistor

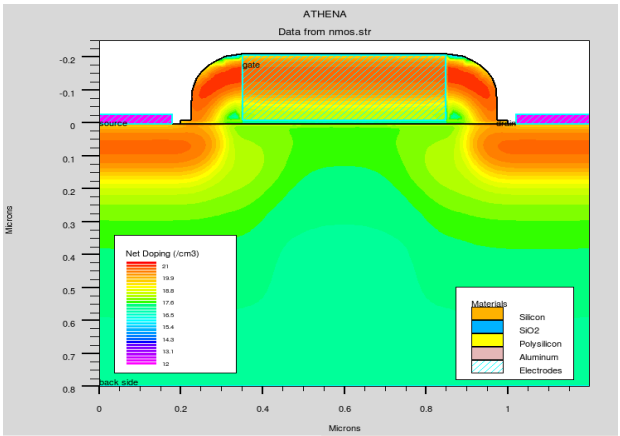

Figure 2: Structure of N N^+ N (junctionless) transistor

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Table 1 Electrode information of junctionless transistor

Electrode name	X min	X max	Y min	Y max
Gate	3.510E-01	8.490E-01	-2.057E-01	-6.336E-03
Source	0.000E+00	1.800E-01	-2.812E-02	4.420E-03
Drain	1.020E+00	1.200E+00	-2.812E-02	4.420E-03
Back side	0.000E+00	1.200E+00	8.000E-01	8.000E-01

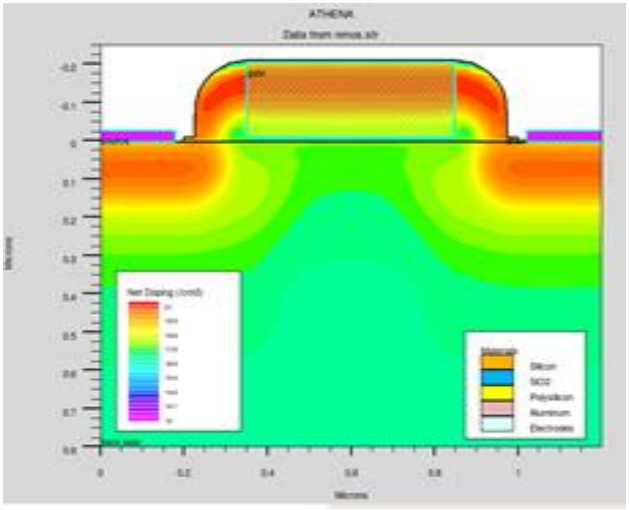

Figure 3: Structure with electrodes N N+ N transistor

Variation of drain current I_d with respect to gate voltage V_g shown in figure (4).as shown in graph when no bias at the i.e. Vg=0.0 there are some current follows through the channel due highly doped drain and source. there are a small current flows from source to drain this small currentmay be called leakage current but this is not in opposite direction of forward bias current, it is in the direction of main current there for this device is also called unidirectional MOS.

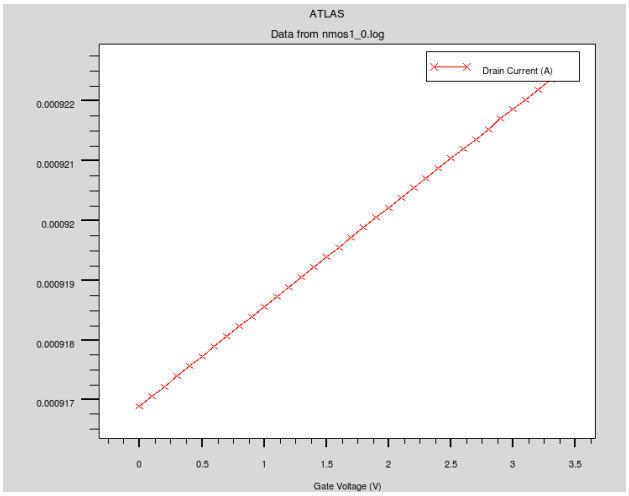

Figure 4: Id Vs Vg plot of 3N transistor

The simulators result shows that the leakage current for N N^+ N transistor is 0.000135843A/µm. which is considerable in amount than convention MOS transistor there for this can be used as an always ON switch for small voltage application.

Positive gate bias Vg > 0

When gate voltage Vg > 0 the drain current Id shown in plot is almost linearly proportional to the gate voltage Vg. The figure (4) shows the variation of Id with Vg varies from 0.0 to 3.3V at constant drain voltage Vd = 1.1V. Therefore 3N transistor is a linear device for small voltage application.

Negative gate bias Vg < 0

From the result of 2D ATLAS simulator threshold voltage (Vt) = ==-515.253 V which is very small as compared to conventional MOS (0.7V for NMOS). Therefore when gate voltage Vt reduced to=-515.253 vV thereafter device turnoff.

Figure (5) shows another characteristics of N N^+ Ntransistor when the polarity of drain and source biasing changes then only the slop of characteristics changes to negative and no other changes occurs , this proves the unidirectional property of N N^+ N transistor.

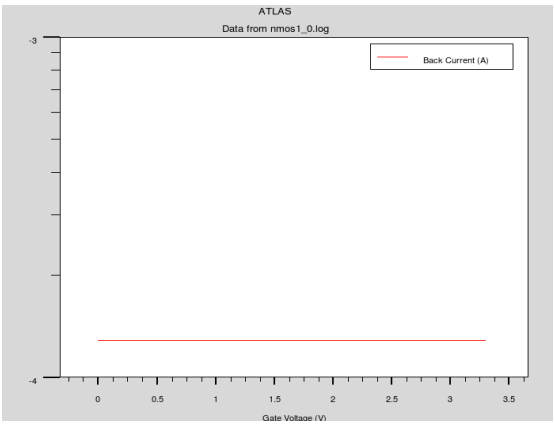

Figure 5: Back current plot of 3N transistor

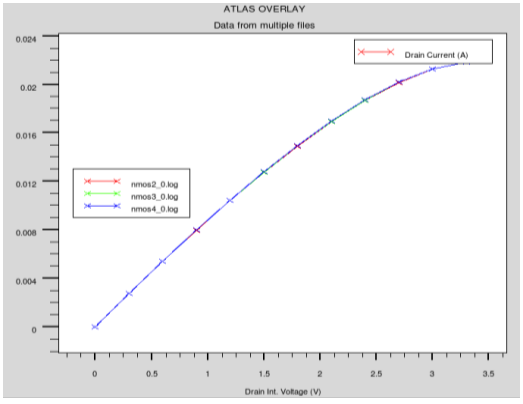

Figure 6: Overlay graph of N N+ N Transistor

4. Comparison with conventional NMOS

N N^+ N transistor and NMOS transistor design with same geometry with gate oxide thickness t_{ox} =0.3µm, gate material thickness = 0.2 µm and channel length = 0.50 µm. are compared from the figure (6) N N^+ N transistor is linear and uni directional and NMOS transistor is linear at 0.5V, after 0.5V device changes to nonlinear and after 1V get saturated.

N N^+ N transistor have very low threshold voltage Vt= =-515.253 V in comparison to NMOS Vt= 0.70V.

And leakage current =0.000135843 A/ µm is smaller than conventional NMOS.

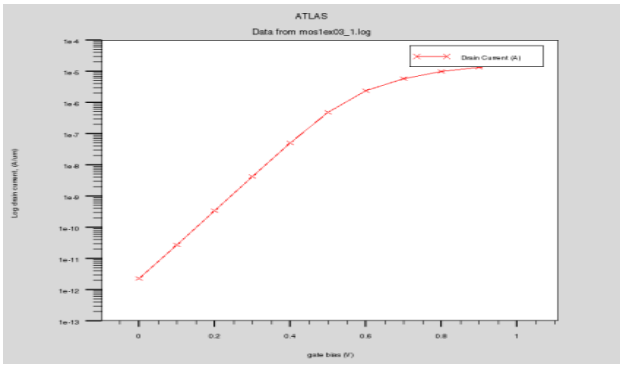

Fig 6.1: Id Vs Vd NMOS

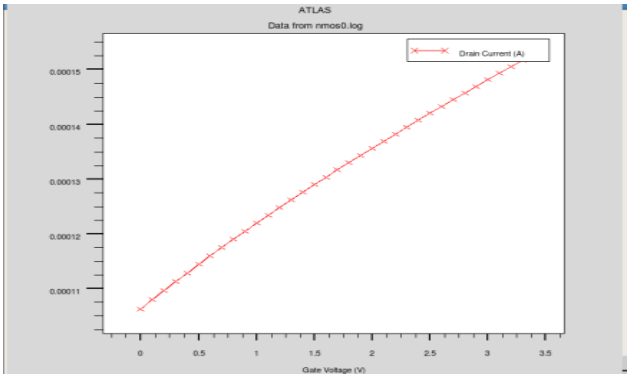

Fig 6.2 Id Vs Vd N^+ N N^+

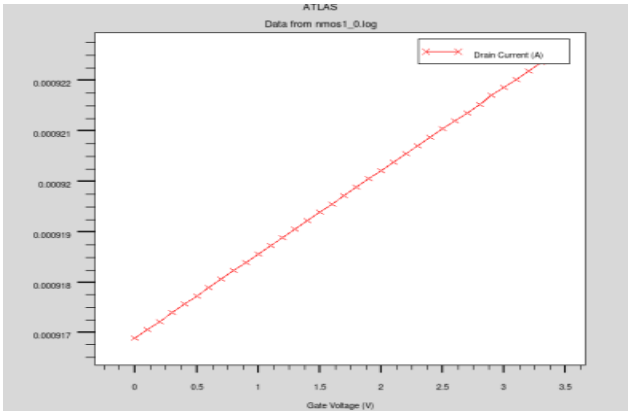

Fig 6.3 Id Vs Vd N N^+ N

Table 2: Compression of various parameter of n n+ n with conventional devices

Parameters	NMOS	N^+ N N^+	N N^+ N
Threshold voltage V_t	0.7V	-6.36619V	-515.253 v
Leakage current	Order of few µm	0.000151693 A/ µm	0.000135843 A/ µm

Conclusion

From the simulator result we can conclude the purposed device is unidirectional, hot carrier and have linear characteristics plot which is very useful for low power switching application and N N^+ N transistor can be used as constant current device for low power application.

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