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Research Article

Low Power Implementation of Sequential Circuits using Reversible Logic Gates

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Abstract

In the recent years, reversible logic has emerged as a promising technology having its applications in low power CMOS, quantum computing, nano technology and optical computing. Reversible logic circuits provide low power dissipation as well as distinct output assignment for each distinct input. The classical gates such as the NAND, AND, NOR, OR, XOR and XNOR are not reversible. This paper demonstrates the reversible logic synthesis Oof sequential circuits. The circuit is designed using only reversible NOT gate, AND/NAND gate, OR/NOR gate and XOR gate. The proposed sequential circuits have been simulated in tanner. The comparative results show that the proposed design is much better in terms of power.

Keywords: *Reversible logic, Reversible gates, CMOS implementation, Flip-flops.*

Introduction

Conventional sequential logic circuits dissipate heat for every bit of information that is lost during their operation. Due to this fact the information once lost cannot be recovered in any way. But the same circuit, if it is constructed using the reversible logic gates will allow the recovery of the information. In 1960s R. Landauer showed that even with high technology circuits using irreversible gates, results in energy dissipation due to information loss (Landauer *et al*, 1961) .He showed that the loss of one bit of information dissipates KTln2 joules of energy where K is the Boltzman's constant and T is the absolute temperature at which the operation is performed. Later Bennett, in 1973, showed that this KTln2 joule of energy dissipation in a circuit can be avoided if it is constructed using reversible logic circuits (Bennett *et al* 1973). Process of running the system both forward and backward has been supported by reversible logic (Perkowski *et al* 2000).This means that reversible computations can generate inputs from outputs and can stop and go back to any point in the computation history.

A circuit is said to be reversible if the input vector can be distinctly recovered from the output vector and there is a one-to-one correspondence between its input and output assignments, i.e. not only the outputs can be distinctly determined from the inputs, but also the inputs can be recovered from the outputs. Information-lossless computation reduces or even eliminates energy dissipation

Motivations

The need for the introduction of reversible logic is that the conventional logic gate dissipates heat due to information loss during operation. Reversible circuits that preserve information, by uncomputing bits instead of throwing them away, will soon offer the only physically possible way to improve the performance. Reversible computing will also lead to improvement in energy efficiency which will increase the speed of circuits such as nanocircuits and therefore the speed of most computing applications.

Reversible Logic

A reversible logic gate is an n-input, n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs but also the inputs can be uniquely recovered from the outputs. Additional inputs or outputs are added so that the numbers of inputs are made equal to the number of outputs whenever it is necessary (Bruce *et al* 2002). A reversible circuit should be designed using minimum number of reversible gates. An essential thing to achieve optimization is that the designed circuit must produce minimum number of garbage outputs; also they must use minimum number of constant inputs (Vasudevan *et al* 2004).

Design of reversible logic gates

Reversible NOT Gate

The NOT gate performs a basic logic function called inversion or complementation. The inverter changes one logic level to its opposite level. In terms of bits, it changes from logic 1 to logic 0 or logic 0 to logic 1. Fig.1 shows CMOS implementation of inverter. If the input is logic 1 it will produce logic 0 as output. If the input is logic 0 it will produce logic 1 as output. Since the number of inputs and output are same it behaves as reversible gate. Therefore

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NOT gate structure is same in both reversible and classical (Abu Sadat *et al* 2010).

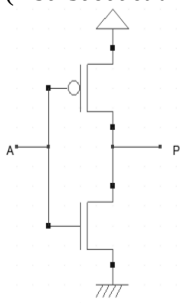

Fig.1 NOT gate

Reversible XOR Gate

A conventional exclusive-OR (XOR) gate takes two single-bit inputs A and B, and yields one single bit output X. If both the inputs are same then the output is logic 0; otherwise the output is logic 1. However, the XOR gate is not reversible, because we cannot uniquely determine what the input vector (B, A) is from the output. For instance, the output logic 1 could have come from one of the two possible input vectors (0, 1) and (1, 0) [6]. Reversible XOR gate has the two single-bit inputs A and B and yields two single-bit output P and Q. Logic symbol of reversible XOR gate is shown in fig.2.

P=A; Q=A B ⊕

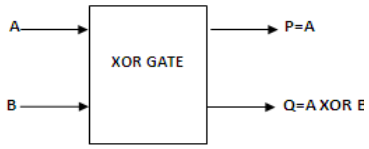

Fig.2 Reversible XOR gate

The Table 1 shows the above function of reversible XOR gate.

Table 1 Truth table of Reversible XOR gate

Input		Output	
A	**B**	**P**	**Q**
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Reversible XOR gate is implemented using CMOS as shown in fig.3

Reversible AND/NAND Gate

Reversible AND/NAND gate has three single-bit inputs A,B,C and three single-bit outputs P,Q,R. Logic symbol of AND/NAND gate is shown in fig 4. If the input C is logic 0 then the circuit work as AND gate. If the input C is logic 1 then the circuit works as NAND gate. The Boolean expression holds good to the conditions of reversibility for AND/NAND gate is P=A; Q=B; R= (A B) ⊕

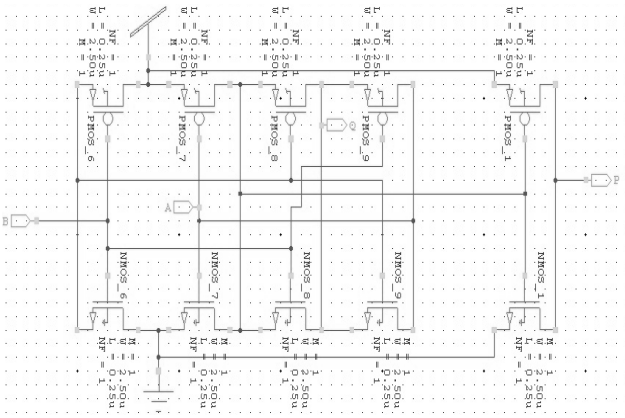

Fig.3 CMOS implementation of reversible XOR gate

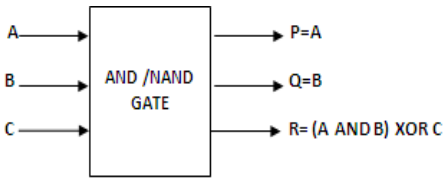

Fig.4 Reversible AND/NAND GATE

The Table 2 shows the above function of reversible AND/NAND gate.

Table 2 Reversible AND/NAND gate

Input			Output		
A	**B**	**C**	**P**	**Q**	**R**
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Reversible AND/NAND gate is implemented using CMOS as shown in fig 5.

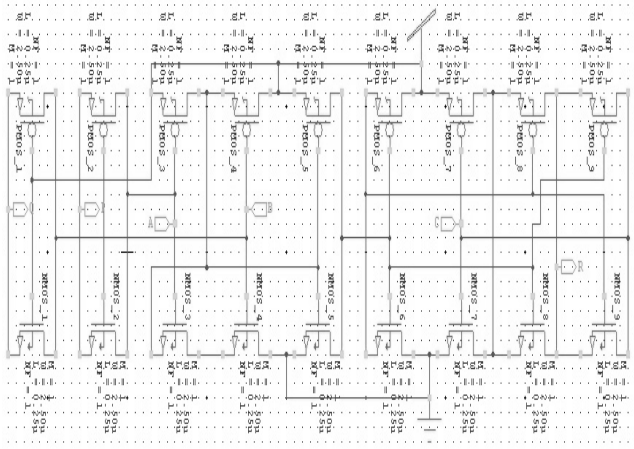

Fig.5 CMOS implementation of Reversible AND/NAND gate

Reversible OR/NOR Gate

Reversible OR/NOR gate needs three single-bit inputs A,B,C and three single-bit outputs P,Q,R. . Logic symbol of OR/NOR gate is shown in fig 4. If the input C is logic 0 then the circuit work as NOR gate. If the input C is logic 1 then the circuit work as OR gate. The Boolean expression holds good to the conditions of reversibility for OR/NOR gate is

P=A; Q=B; R= (A OR B)' XOR C

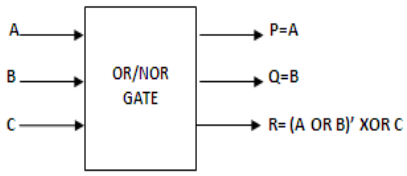

Fig 6 OR/NOR gate

The Table 3 shows the above function of reversible OR/NOR gate.

Table 3 OR/NOR gate

Input			Output		
A	**B**	**C**	**P**	**Q**	**R**
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	1	0

CMOS implementation of Reversible OR/NOR gate is shown in fig 7.

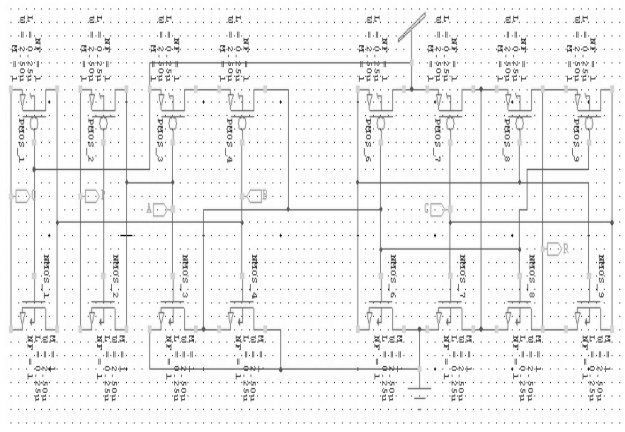

Fig 7 CMOS implementation of OR/NOR gate

Proposed Flip-Flop Design

Flip flops are the basic building blocks of sequential circuits. Flip flop is a circuit that has two states and used to store single bit of information. In flip flops state changes takes place depending on the clock signal.Clocking causes the flip-flop to either change or retain its output signal based upon the values of the input signals at the transition. There are four basic flip flops. They are

- D flip flop
- T flip flop
- SR flip flop
- JK flip flop

D- Flip-flop

D flip-flop is widely used. It is also known as "data" or "delay". D flip-flop has one data input D and clock input. D flip-flop is designed using reversible AND/NAND gate as shown in fig 8. If the clock is high whatever input given to D is produced at the output (Hari *et al* 2006). Truth table of D flip-flop is given table 4.

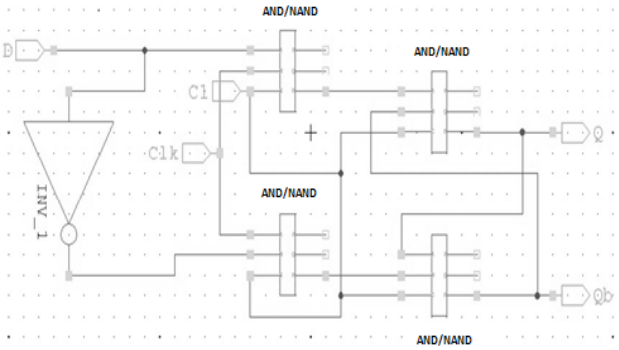

Fig 8 D flip-flop

Table 4 D flip-flop

Clk	D	Q	Q'
low	X	No change	
High	0	0	1
High	1	1	0

SR- Flip-flop

SR flip-flop has two inputs set and reset. This flip-flop is designed using reversible AND/NAND gates as shown in fig 9. Truth table of SR flip-flop is shown in table 5.

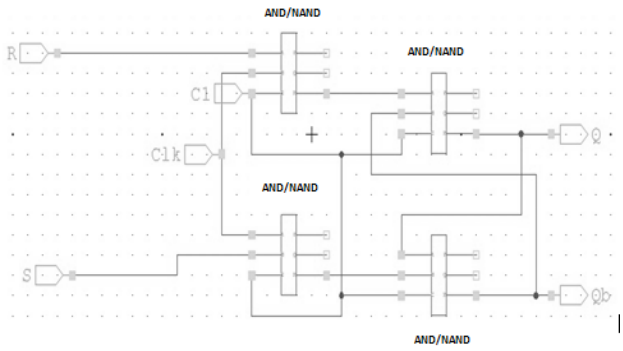

Fig 9 SR flip-flop

Table 5 SR flip-flop

Clk	S	R	Q_{n+1}
High	0	0	Q_n
High	0	1	0
High	1	0	1
High	1	1	undeterminate

JK- Flip-flop

This simple **JK flip Flop** is the most widely used of all the flip-flop designs the sequential operation of the JK flip flop is exactly the same as for the previous SR flip-flop with the same "Set" and "Reset" inputs (Mozammel *et al* 2011). The difference this time is that the "JK flip flop" has no invalid or forbidden input states of the SR Latch even when S and R are both at logic "1″. This flip-flop is designed using reversible AND/NAND gate as shown in fig 10 . truth table is shown in table 6.

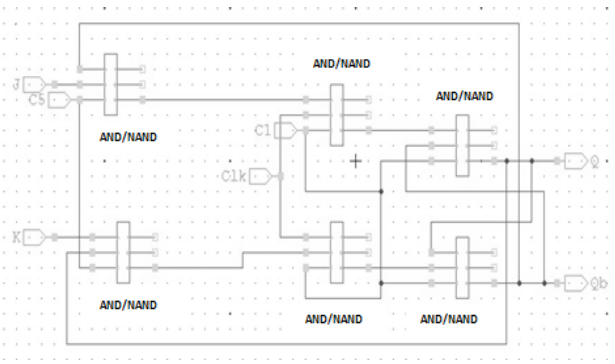

Fig 10JK Flip-flop

Table 6 JK flip-flop

Clk	J	K	Q_{n+1}
High	0	0	Q_n
High	0	1	0
High	1	0	1
High	1	1	Q_n '

T- Flip-flop

T flip-flops are similar to JK flip-flops. T flip-flops are single input version of JK flip-flops. This modified form of JK flip-flop is obtained by connecting both inputs J and K together. This flip-flop is designed using reversible AND/NAND gate, OR/NOR gate, XOR gate as shown in fig 11. This flip-flop has only one input along with Clock pulse. These flip-flops are called T flip-flops because of their ability to complement its state (i.e.) Toggle (Rajmohan *et al* 2011). So they are called as Toggle flip-flop. Truth table is shown in table 7.

Table 7 T flip-flop

Clk	T	Q	Q'
low	X	No change	
high	0	1	0
high	1	Toggle	

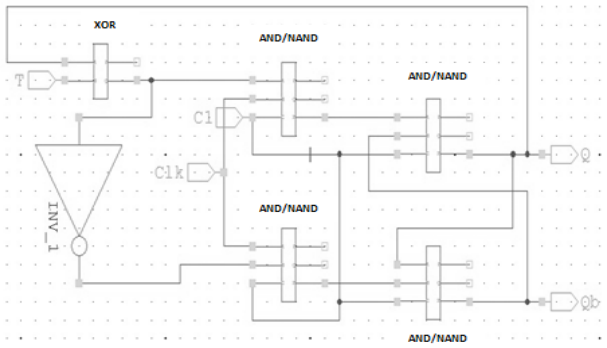

Fig 11 T flip-flop

Power Analysis

Power consumed by the sequential circuits using reversible logic gates is compared with the power consumed by the sequential circuits designed using classical logic gates as shown in table 8.

Table 8 Power comparison

Flip-Flops	Classical	Reversible
D FLIP-FLOP	2.5130e-002 watts	8.2112e-003watts
SR FLIP-FLOP	2.3304e-002 watts	5.9650e-003watts
JK FLIP-FLOP	3.1353e-002 watts	1.2344e-003watts
T FLIP-FLOP	2.6677e-002 watts	7.9017e-003wats

Conclusion

In this paper, we have designed the sequential circuits using reversible logic gates. The proposed system consumes less power than the existing sequential circuits designed using classical logic gates. Thus the proposed sequential circuit can be used in low power CMOS application.

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